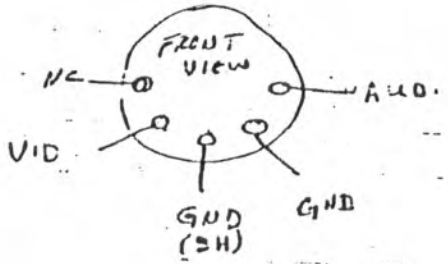
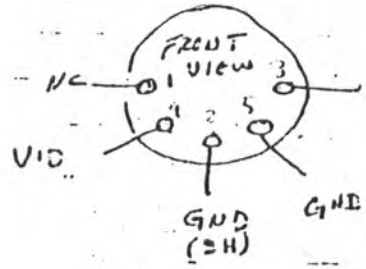


Box #1

CABLE #	# of cables
1	1
2	2
3	3
4	3
5	2
6	1

GND
GND
GND
GND



#1 — N.C.

2. — Video Ground

3 — Audio

4 — Video

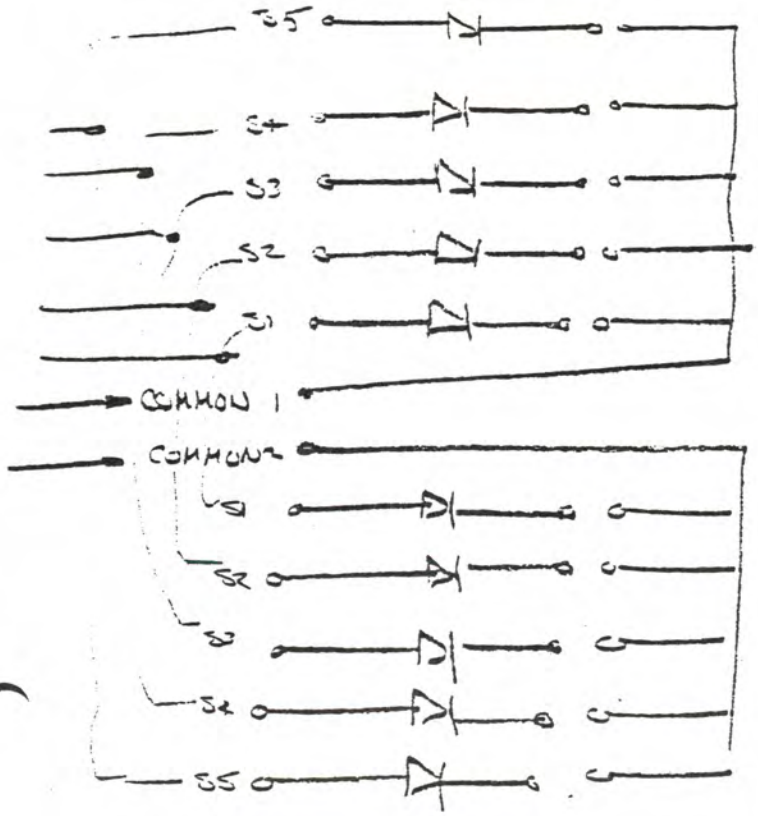
5 — Audio Ground

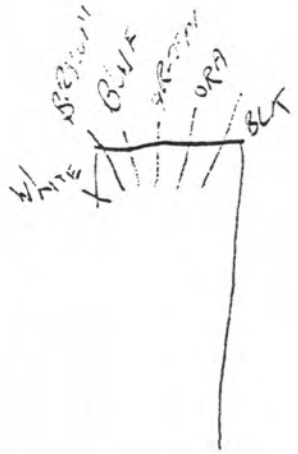
GND
GND
GND
GND

Memo
from

JIM SHAH

JOY STICKS





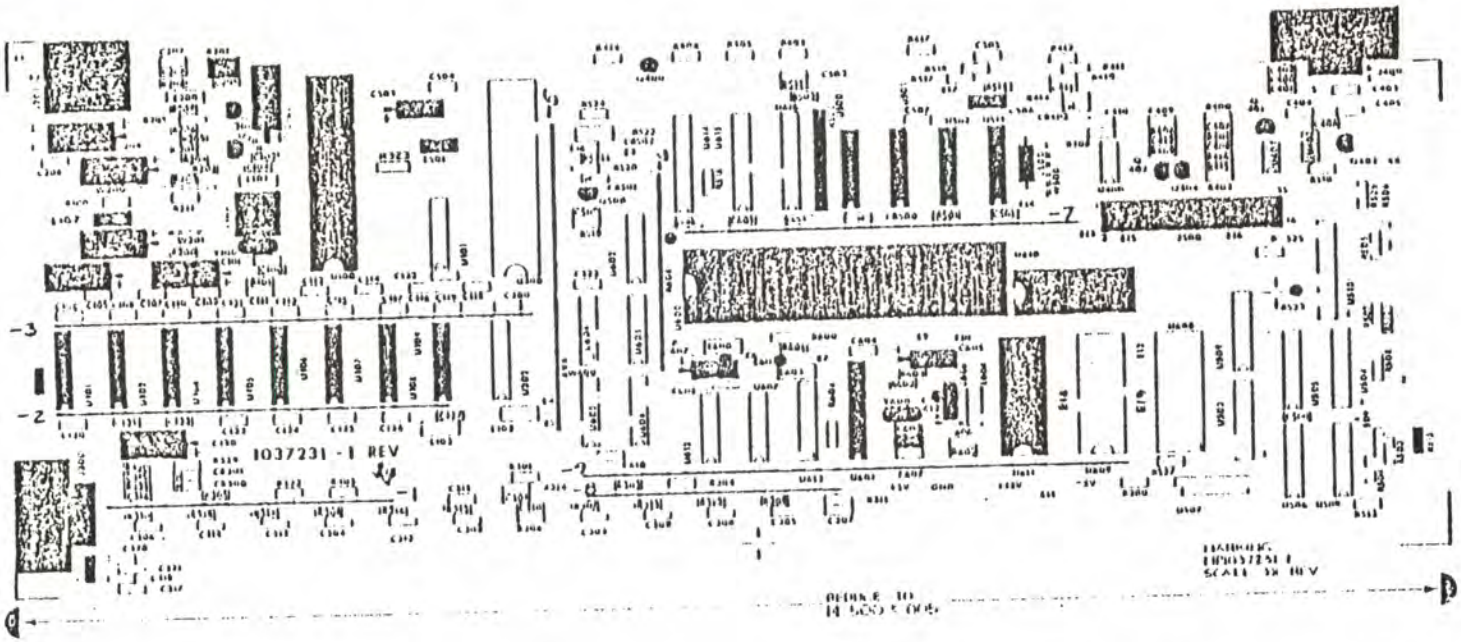
TEXAS INSTRUMENTS
INCORPORATED
P. O. BOX 10508 • MAIL STATION 5853 • LUBBOCK, TEXAS 79408
806 / 741-2882

Problem Area of Cassette Interface

1. Reliable Recovery of data is dependent on Recorder used during save.
2. Reliability is directly proportional to FREQ RESPONSE of CASSETTE DECK.
   may allowed. 2.5 KHz ± 3DB.
3. Reliability can be observed by Looking for the "EYE" or "Jitter"
   Phenomenon with an oscilloscope.
   A. our present reliability is dependent on ammount of JITTER.
      IF Jitter < 60 μs cassette should work.
4. Cassette is also adversely affected by speed changes.
   A. our motor control circuit can under special circumstances cause this.

HOME Computer Cassette Interface

1. Operates with Byte/Manchester Encoding Format.
2. Utilizes Redundancy to gain increased reliability.
3. USES WAVE SHAPING ON Input and Output to Increase Reliability
4. HAS Two motor Control circuits which allow computer to control decks
5. HAS CAPABILITY of Reading from one deck and writing to another, under computer control.
6. The interface is software intensive and relies on 9901 interval timer for it's timing



SOCKETS

16 PIN - U101, U102, U104, U105, U106, U107, U108, U109, U500, U501, U502, U511
20 PIN - U601
24 PIN - U610, U611
40 PIN - U100

ICs

U101 - TMS 4116
U102 - TMS 4116
U104 - TMS 4116
U105 - TMS 4116
U106 - TMS 4116
U107 - TMS 4116
U108 - TMS 4116
U109 - TMS 4116
U500 - TMC 0430
U501 - TMC 0430
U502 - TMC 0430
U511 - TMC 9919
U601 - 74LS362
U610 - TMS 4732
U611 - TMS 4732
U100 - TMC 9918
U600 - TMS 9900
U401 TL117
U402 TL117

CRYSTALS

Y100 - 10.7 MHz
Y600 - 48. MHz

INDUCTORS

L100 - 2-4.5 uH (TUNABLE)
L107 - SELF RESONATOR
L500 - 6.8 uH
L501 - 6.8 uH
L602 - .33 uH

CONNECTORS

J201 - 5 PIN VIDEO CONN.
J300 - 9 PIN CASSETTE CONN.
J400 - 9 PIN CASSETTE CONN.
J500 - 18 PIN DOUBLE ROW EDGE CONN.

CAPACITORS

C103 - .100uF
C128 - 125uF
C129 - 125uF
C130 - 125uF
C133 - 68 pF
C200 - 100uF
C202 - 100uF
C204 - 220uF
C219 - .001uF
C503 - 100uF
C506 - 22uF
C600 - 100uF
C605 - 10uF
C606 - 22uF
C611 - .001uF
C612 - .1uF

TRANSISTORS

Q200 - AST3904
Q201 - AST3904
Q400 - TIS92
Q401 - TIS92
Q402 - TIS92
Q403 - TIS92
Q404 - TIS92
Q500 - TIS92

BUSS BARS

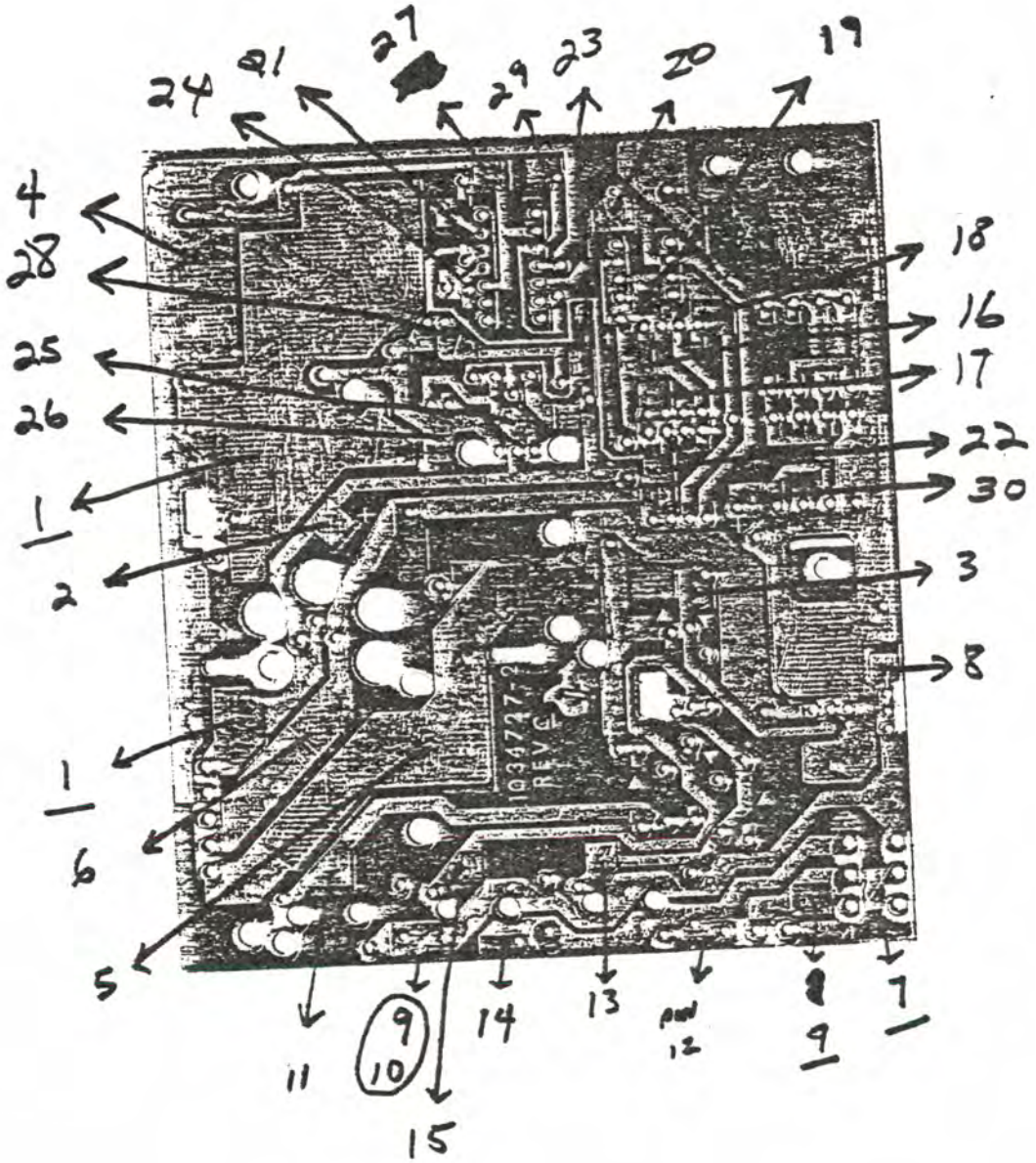
-1
-2
-3
-5
-6
-7
-8
-9

RESISTORS

R323 - 10KΩ
R600 - 10KΩ RES. PAK
R615 - 1KΩ
R523 - 100Ω
R607 - 4.7KΩ
R608 - 1KΩ

POT

R201 - 2.5K


24
21
27
29
23
20
19
4
28
25
26
1
2
1
6
5
11
9
10
15
14
13
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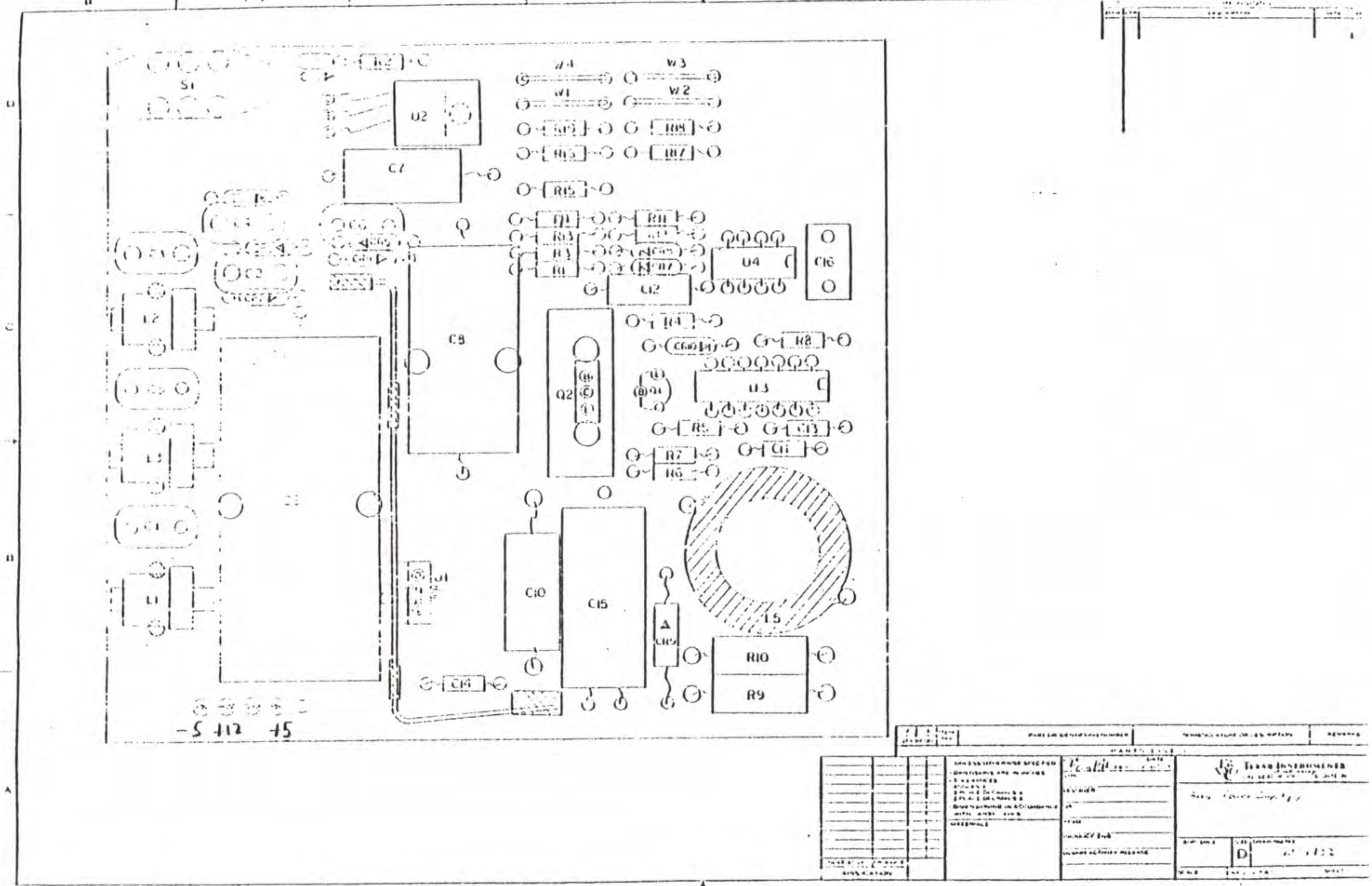
7
18
16
17
22
30
3
8
103727-2
REV G


S1
U2
C7
W4
W3
W1
W2
R15
C8
Q2
U4
C16
U3
R8
R5
R7
C10
C15
L5
R10
R9
L2
L3
L1
-5 +12 +5
TEXAS INSTRUMENTS
D

TEXAS INSTRUMENTS
INCORPORATED

HOME COMPUTER

FINAL TEST

TITLE				
H.C. FINAL TEST (PRELIMINARY)	SH 1 OF 7	DWG A SIZE	Flores 7-23-79	7 23 79

INSTRUCTIONS:

1. EQUIPMENT NEEDED

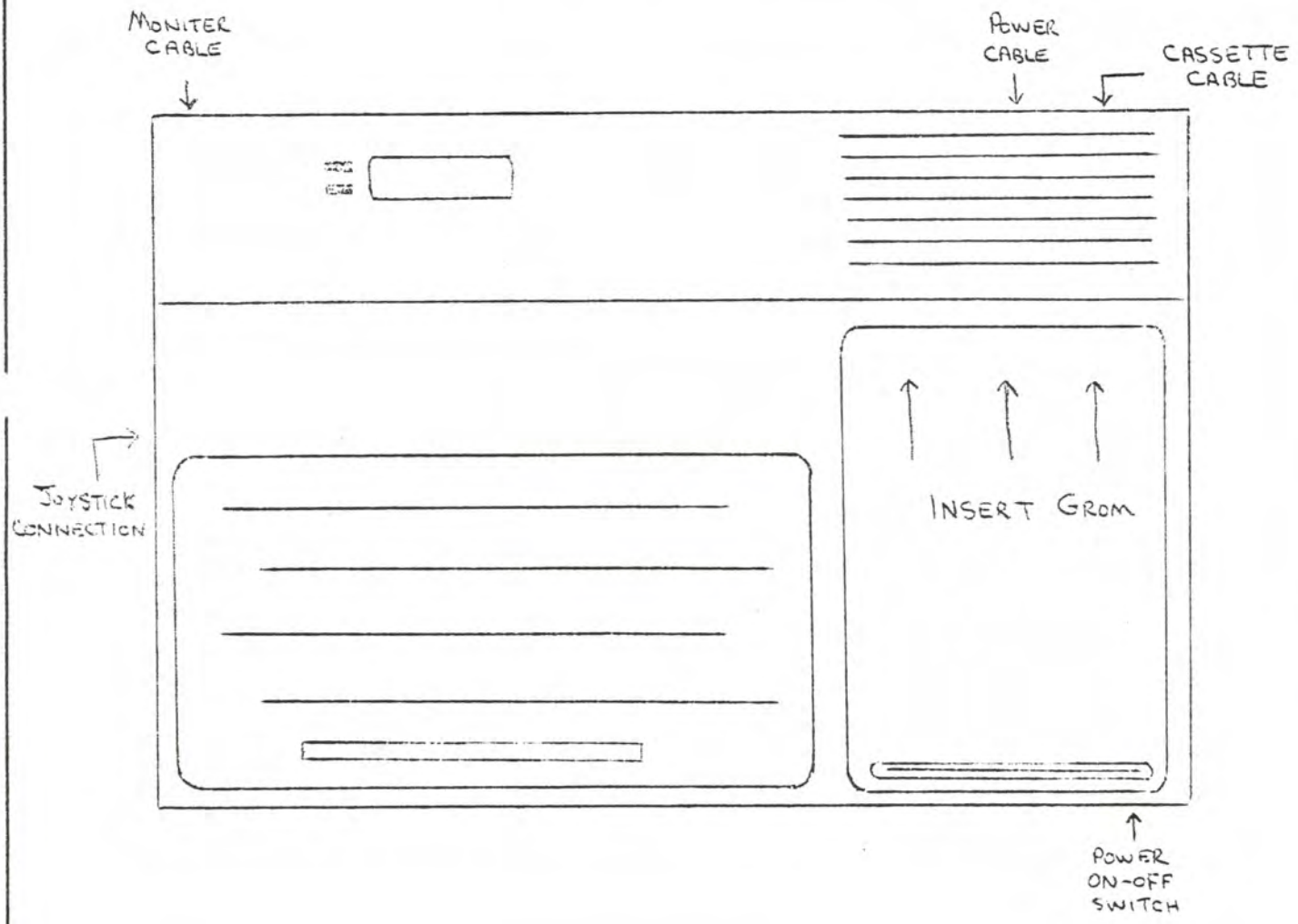
   a. 1 ZENITH COLOR MONITER
   b. 1 MONITER CABLE
   c. 1 DIAGNOSTIC GROM
   d. 1 JOYSTICKS PERIPHERAL
   e. 1 CASSETTE PLAYER/RECORDER
   f. 1 CASSETTE CABLE
   g. 1 BLANK CASSETTE TAPE

NOTE: ON G.E. CASSETTE PLAYER, THE TONE SHOULD BE AT LEVEL 4 AND THE VOLUME LEVEL BETWEEN 3 AND 4.
ON PANASONIC CASSETTE PLAYER, THE TONE SHOULD BE AT LEVEL 10 AND THE VOLUME LEVEL AT 5.

INSTRUCTIONS:

1. CONNECT POWER CABLE FROM WALL TRANSFORMER
2. CONNECT PERIPHERAL CABLES: a) COLOR MONITER CABLE
   b) CASSETTE CABLE
   c) JOYSTICK CABLE
3. INSERT DIAGNOSTIC GROM

PICTORIAL: HOME COMPUTER TOP VIEW



TITLE				
H.C. FINAL TEST	SH 3 OF 7	DWG A SIZE	Flores	7-23-79

INSTRUCTIONS :	RESULTING MONITER SCREEN
1. POWER UNIT ON	TI LOGO
2. PRESS '3'	OPERATION MENU
3. PRESS '3'	DIAGNOSTIC TESTS LOGO
4. PRESS '3'	DIAGNOSTIC TEST MENU
5. PRESS '1'	*KEYBOARD TEST*
6. ROLL 1 FINGER ACROSS TOP ROW OF KEYS THEN PRESS SPACE BAR TWICE, ROLL FINGER ACROSS SECOND ROW OF KEYS THEN PRESS SPACE BAR TWICE, ROLL FINGER ACROSS THIRD ROW OF KEYS THEN PRESS SPACE BAR TWICE ROLL FINGER ACROSS BOTTOM ROW OF KEYS SCREEN SHOULD APPEAR AS SHOWN ON RIGHT.	1 2 3 4 5 6 7 8 9 0 Q W E R T Y U I O P A S D F G H J K L ↑Z X C Y B N M . ENT
NOTE : CHECK FOR STICKING KEYS, STICKING SPACE BAR, & KEYS NOT ENTERING DURING KEYBOARD TEST.	
7. PRESS "ENTER"	DIAGNOSTIC TEST MENU

INSTRUCTIONS:

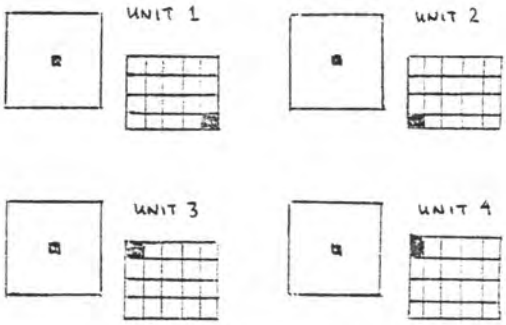
RESULTING MONITER SCREEN:

DIAGNOSTIC TEST MENU

*HANDSET TEST *

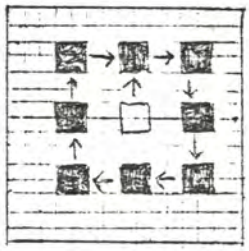
1. PRESS '7'

2. PRESS 'V' AND 'B'



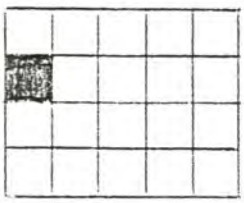
NOTE: CHECK THE POSITION OF THE DARK SQUARE WITHIN THE SMALL RECTANGLE IN UNITS 1 & 2.

3. ROTATE THE JOYSTICK HANDLES TO MOVE THE DARK SQUARE WITHIN THE LARGE SQUARE TO THE EIGHT POSITIONS SHOWN AT RIGHT



NOTE: TEST SHOULD BE FOR BOTH UNITS 1 & 2.

4. PRESS ORANGE BUTTON ON BOTH JOYSTICK CONTROLLERS.



NOTE: CHECK THE POSITION OF THE DARK SQUARE WITHIN THE SMALL RECTANGLE IN UNITS 1 & 2. POSITION SHOULD BE AS SHOWN AT RIGHT.

5. PRESS "ENTER"

6. PRESS "ENTER"

DIAGNOSTIC TEST MENU

INSTRUCTIONS:	RESULTING MONITER SCREEN:
	DIAGNOSTIC TEST MENU
1. PRESS '6'	CASSETTE TEST MODE (CS1 or CS2)
2. PRESS '2' NOTE: FOLLOW INSTRUCTIONS ON THE SCREEN	* CASSETTE TEST * REWIND TAPE, THEN PRESS ENTER PRESS CASSETTE RECORD, THEN PRESS ENTER RECORDING PRESS CASSETTE STOP, THEN PRESS ENTER CHECK TAPE (Y OR N)?
3. PRESS 'Y' NOTE: FOLLOW INSTRUCTIONS ON THE SCREEN	REWIND TAPE, THEN PRESS ENTER PRESS CASSETTE PLAY, THEN PRESS ENTER READING
4. AFTER READING: IF SCREEN IS..... FOLLOW INSTRUCTIONS AND GO TO STEP 5.	DATA OK PRESS CASSETTE STOP, THEN PRESS ENTER
IF SCREEN IS..... PRESS 'R', AND GO TO STEP 2 AFTER 2 READINGS, IF SCREEN IS THE SAME, UNIT FAILS CASSETTE.	ERROR: NO DATA FOUND, OR ERROR IN DATA FOUND

NOTE: IN STEPS 2 & 3, AFTER PRESSING CASSETTE RECORD & CASSETTE PLAY, CHECK IF CASSETTE IS MOVING BEFORE 'ENTER' IS PRESSED. IF IT DOES, UNIT FAILS CASSETTE MOTOR CONTROL.

5. PRESS 'ENTER'	DIAGNOSTIC TEST MENU

INSTRUCTIONS:	RESULTING MONITER SCREEN:
	DIAGNOSTIC TEST MENU
1. PRESS '9' NOTE: RUN 1 CYCLE OF AUTOMATIC TEST. CYCLE IS COMPLETED WHEN *RAM TEST* APPEARS AFTER CALCULATION TEST.	* RAM TEST* SPRITE TEST VIDEO TEST * SOUND TEST* * CALCULATION TEST* * RAM TEST *
2. PRESS "SPACE" KEY NOTE: IF NO ERRORS SHOWN ON MONITER SCREEN, GO TO STEP 3. IF ERRORS ARE NOTED ON MONITER SCREEN, UNITS FAILS FOR NOTED ERRORS.	
3. PRESS 'ENTER'	DIAGNOSTIC TEST MENU
4. POWER UNIT OFF	
5. DISCONNECT ALL CABLES AND GROM	
6. TEST COMPLETED	

Tenario

Cecil Farris

MEMORANDUM

October 17, 1979

TO: Cecil Farris
Jan Pailes
Gary LaGrange
Pat Kiefer
Dan Wikander
Nick Flores

COPY: Lee Kitchens
Omar Duffer
Al Coe
Rex Naden

FROM: Byron Crowe

SUBJECT: MAINFRAME BURN-IN PROCEDURE

Attached is a revised copy of the Burn-in procedure for both new and retrofited mainframes. Short cycle post burn-in requirements are added for the first time. Please mark up a copy showing changes you feel are needed, and return to me. Several revisions will probably be required in coming weeks. I plan to meet with Q.C. and Manufacturing before 10/18 to discuss this procedure and define failure systoms and terminology to be used.

Thank You.

Byron Crowe

Byron Crowe
JBC:er

(1) Copy Rex Sent

(2) RTP

BURN IN TEST PROCEDURE

NOTE: All Burn-In units will run QRA Test for 48 hours, and GROM Diagnostic Test for 48 hours.

1. QRA BASIC TEST INSTRUCTIONS

   a. Connect monitor cable, transformer cable, and cassette cord to H/C unit.

   b. Power unit "ON". Monitor screen should have TI Logo.

   c. Press '1' twice. Monitor screen should have "TI BASIC READY"

   d. Enter "OLD CS1". Then press "enter" key.

   e. Follow instructions on screen .....
      * Rewind cassette tape, then press enter
      * Press cassette play, then press enter reading

   f. After reading if screen is .....
      follow instructions and go to step g.
      * Data OK
      * Press cassette stop, then press enter

      if screen is .....
      press "R" and go to step e. After 2 readings if results are the same, unit has cassette read problem.
      * ERROR: No data detected or error detected in data.

NOTE: Check volume & tone levels and cassette cord connections.

   g. Enter "Run". Then press "enter" key.

   h. After 1 cycle of test is complete, enter '10000' and press "enter" key when "Enter Test Cycles Desired" appears.

   i. To check time, press 'shift' key and 'C' at same time. Then enter 'Print T' and press 'enter' key. Number of cycles should appear on screen. ~~Record number of cycles completed on B.I. Log.~~
      Enter 'CON' and press enter key to resume test.

NOTE: If H/C unit is not running test or if an error has been detected in program, list the status of unit and the number of cycles completed (if possible) on History Card. Any Soft failure (lock-up) should be moved to engineering rack and restarted at 0 time. Any Hard failure should be sent to Burn-In TS&R, after which it will go to a designated rack for TS&R Burn-In.

BURN-IN TEST PROCEDURE
cont.

j. When H/C unit has completed 2400 cycles of QRA Test (approx. 46 hours) unit is to be verified by QC, who will then update the history card and turn unit "OFF" for a cool down of at least one (1) hour before beginning the GROM Diagnostic Test.

2. GROM DIAGNOSTIC QRA TEST INSTRUCTIONS

a. Power unit "ON". Monitor screen should have TI Logo.

b. Insert GROM Diagnostic Command Module. Monitor screen should have TI Logo with French wording.

c. Press '3' three times (slowly) for RAM Test from Diagnostic screen.

d. Press '5' once for Column Disturb RAM Test.

e. Press '2' once for Loop Testing.

f. To check for accummulative time and errors:
Press space bar once and note test time and errors on History Card and Burn-In Log.

NOTE: Test time is given in Hrs: MIN: SEC.

NOTE: If an error is detected: AFTER 96 HOURS Any Soft (lock-up) failure should be moved to Engineering Rack and restarted at 0 time. Any Hard failure should be sent to Burn-In TS&R, after which it is to go on a designated TS&R Burn-In Rack.

g. Press space bar again to resume test.

h. When unit test time is 46 hours, QC will again verify time and update History Card, and test is completed.

3. SHORT CYCLE BURN-IN REQUIREMENTS

When a unit has completed the normal 96 hour burn-in cycle, but has afterward undergone TS&R, the following requirements apply:

a. MLB removed and electronic component replaced or soldering involved: --Full 96 hour burn-in.

b. MLB removed from top case, but shields not removed: --24 hours burn-in with diagnostic GROM.

c. Power supply TS&R: --Full 96 hour burn-in.

d. VLED replaced on power supply: --No additional burn-in.

Byron Crowe 10/17/79

T I 9 9 / 4 T E S T S E T E R R O R T A B L E

FAILURE #	ERROR MSG	ERROR PARAMETER	ALLOWED VALUES HIGH	LOW	TABLE #
0	SYSTEM VOLTAGE	GROM +5 V	1075	972	1
		I/O +5 V	1075	972	2
		VIDEO +12 V	1283	1049	3
		GROM -5 V	- 972	- 1075	4
		I/O -5 V	- 972	- 1075	5
		GROM GROUND	- 61	- 225	6
1	SYSTEM CLOCK	I/O 3.0 MHZ	30009	29991	7
		GROM CLOCK	4800	4400	8
12	CASS. MOTOR CONTROLS	CS1 ON	350	0	9
		CS1 OFF	1076	972	10
		CS2 ON	358	0	11
		CS2 OFF	1076	972	12
13	CASS. OUTPUT	OUTPUT ON	1116	372	13
15	AUDIO GATE	OFF (VIDEO)	10	0	14
		ON (VIDEO)	310	290	15
18	9919 TONE BAD	9919 REG 0 VID	115	105	16
		9919 REG 1 VID	115	105	17
		9919 REG 2 VID	115	105	18
		9919 REG 0 EAR	115	105	19
		9919 REG 1 EAR	115	105	20
		9919 REG 2 EAR	115	105	21
19	9919 TONE BAD	9919 REG 0 VID	14683	13285	22
		9919 REG 1 VID	14683	13285	23
		9919 REG 2 VID	14683	13285	24
20	TONE ATTEN.	REG 0 0 DB	1590	530	25
		REG 1 0 DB	1590	530	26
		REG 2 0 DB	1590	530	27
21	TONE ATTEN.	REG 0 - 2 DB	1044	348	28
		REG 1 - 2 DB	1044	348	29
		REG 2 - 2 DB	1044	348	30
22	TONE ATTEN.	REG 0 - 4 DB	699	233	31
		REG 1 - 4 DB	699	233	32
		REG 2 - 4 DB	699	233	33
23	TONE ATTEN.	REG 0 - 8 DB	400	119	34
		REG 1 - 8 DB	400	119	35
		REG 2 - 8 DB	400	119	36

FAILURE #	ERROR MSG	ERROR PARAMETER	ALLOWED VALUES HIGH	LOW	TABLE #
24	TONE ATTEN.	REG 0 -16 DB	181	61	37
		REG 1 -16 DB	181	61	38
		REG 2 -16 DB	181	61	39
25	TONE ATTEN.	REG 0 OFF	25	-25	40
		REG 1 OFF	25	-25	41
		REG 2 OFF	25	-25	42
26	NOISE ATTEN.	WHITE 0 DB	2443	815	43
		WHITE - 2 DB	2392	798	44
		WHITE - 4 DB	1924	642	45
		WHITE - 8 DB	1222	408	46
		WHITE -16 DB	412	138	47
		WHITE OFF	25	-25	48
		PERIOD 0 DB	2443	815	49
		PERIOD - 2 DB	2392	798	50
		PERIOD - 4 DB	1924	642	51
		PERIOD - 8 DB	1222	408	52
		PERIOD -16 DB	412	138	53
		PERIOD OFF	25	-25	54
27	EXTERNAL AUDIO	I/O PORT	1253	1133	55
		CASSETTE PORT	1253	1133	56
28	AUDIO SUMMING	1 REG ON	160	54	57
		2 REG ON	402	134	58
		3 REG ON	847	283	59
		4 REG ON	1176	392	60
		4 REG + EXT	1882	628	61
--	UUT NOISE HIGH	TESTER CALIB	410	---	--

NOTE : ON AN ERROR, THE TEST SET WILL ABORT THE REMAINING MEASUREMENTS FOR THE TEST CURRENTLY IN PROGRESS, WITH THE UNMEASURED PARAMETERS LISTED WITH A 0 VALUE.

THE TWO NUMBERS LISTED AFTER AN ERROR PRINTOUT INDICATE THE TABLE # AND THE ACTUAL PARAMETER MEASUREMENT OF THE LAST ADC OR COUNTER CYCLE. THESE MAY OR MAY NOT BE ASSOCIATED WITH THE ERROR.

(.PAULH.HOMF.PARLST)

TI 99/4 TEST SET #2

PARAMETER TABLE

FAILURE #	ERROR MSG	ERROR PARAMETER	ALLOWED VALUES HIGH	LOW	TABLE #
0	POWER SUPPLY	I/O +5	1050	1010	1
		GROM +5 V	1050	1010	2
		I/O -5 V	- 950	- 1050	3
		GROM -5 V	- 950	1050	4
		VIDEO +12/2 V	1260	1140	5
		GROM GROUND	- 120	- 220	6
1	UUT CLOCKS	I/O 3.0 MHZ	30300	29700	7
		GROM CLOCK	4476	4473	8
10	MOTOR CNTL 1	CS1 ON	520	0	9
		CS1 OFF	1050	950	10
	MOTOR CNTL 2	CS2 ON	520	0	11
		CS2 OFF	1050	950	12
11	CASS. OUTPUT	OUTPUT ON	1640	720	13
13	AUDIO GATE	OFF (EARPH.)	10	0	14
		ON (EARPH.)	315	295	15
14	CASS AUDIO	INPUT ON	1020	990	16
	I/O EXT AUDIO	INPUT ON	1020	990	17
18	TONE FREQ	REG 0 (EARPH)	118	102	18
		REG 1 (EARPH)	118	102	19
		REG 2 (EARPH)	118	102	20
		REG 0 (EARPH)	14683	13285	21
		REG 1 (EARPH)	14683	13285	22
		REG 2 (EARPH)	14683	13285	23
19	TONE ATTEN. (VIDEO)	REG 0 0 DB	-----	900	24
		REG 0 - 6 DB	^ = .7079	----	25
		REG 0 -12 DB	^ = .7079	----	26
		REG 0 -18 DB	^ = .7079	----	27
		REG 0 -24 DB	^ = .7079	----	28
		REG 1 0 DB	-----	900	29
		REG 1 - 6 DB	^ = .7079	----	30
		REG 1 -12 DB	^ = .7079	----	31
		REG 1 -18 DB	^ = .7079	----	32
		REG 1 -24 DB	^ = .7079	----	33
		REG 2 0 DB	-----	900	34
		REG 2 - 6 DB	^ = .7079	----	35
		REG 2 -12 DB	^ = .7079	----	36
		REG 2 -18 DB	^ = .7079	----	37

20	WHITE NOISE	0 DB (VID)	------	900	39
		- 6 DB (VID)	^ = .8912	---	40
		-12 DB (VID)	^ = .7943	---	41
		-18 DB (VID)	^ = .7943	---	42
		-24 DB (VID)	^ = .7943	---	43
	PERIOD. NOISE	0 DB (VID)	------	900	44
		- 6 DB (VID)	^ = .8912	---	45
		-12 DB (VID)	^ = .7943	---	46
		-18 DB (VID)	^ = .7943	---	47
		-24 DB (VID)	^ = .7943	---	48
21	AUDIO SUMMING (VIDEO)	ALL ON (REF)	------	900	49
		4 REG ON / REF =	.955	.479	50
		3 REG ON / REF =	.881	.442	51
		2 REG ON / REF =	.462	.232	52
		1 REG ON / REF =	.216	.108	53

NOTE : THIS LIST IS TO BE USED WHEN AN ERROR PRINTOUT IS OF THE FORM :

```
  *FAILURE*
STEP # nnnn

 (text message)

 AA
 BBBB
```

AA = POSITION IN TABLE (TABLE #)
BBBB = ACTUAL MEASURED VALUE

COMPARISON OF THE MEASURED VALUE WITH THE LISTED HIGH AND LOW ALLOWED VALUES WILL REVEAL WHY THE ERROR WAS PRINTED.

(U.PAULH.T994A.PARLST)

9 9 / 4 F A I L U R E A N A L Y S I S

FOR USE WITH TEST SET ERROR PRINTOUTS

I PRINTOUT EXPLANATION

WHEN THE 99/4 TEST SET DETECTS A UUT FAILURE, AN ERROR MESSAGE IS PRINTED DESCRIBING THE FAILURE SYMPTOM. IN ADDITION, TWO NUMBERS ARE PRINTED DESIGNATING THE LAST MEASURED PARAMETER (USING THE TEST SET`S ADC OR FREQUENCY COUNTER). THIS PRINTOUT CAN BE USED, ALONG WITH THIS DOCUMENT AND THE `TEST SET ERROR TABLE`, TO DETERMINE WHAT NEEDS TO BE REPAIRED IN THE UUT. AN EXAMPLE PRINTOUT FOLLOWS :

```
 * FAILURE *
STEP # AA          AA = TEST NUMBER OF FAILURE

SAMPLE MESSAGE     DESCRIPTION OF FAILED TEST
BB                 BB = PARAMETER NUMBER IN ERROR TABLE
CCCCC              CCCCC = ACTUAL PARAMETER MEASUREMENT
```

THE LAST TWO ITEMS PRINTED (ERROR TABLE INFO) ARE PRINTED FOR EVERY FAILURE, REGARDLESS OF WHETHER THAT PARAMETER WAS MEASURED FOR THAT TEST OR FOR A PREVIOUS ONE. THUS, THERE WILL BE CASES WHEN THE ERROR TABLE INFO SHOULD BE DISREGARDED. ONLY FOR THOSE ERRORS APPEARING IN THE ERROR TABLE DOCUMENT WILL THE PARAMETER INFORMATION BE MEANINGFUL.

II IF AN ERROR OCCURS DURING A TEST, THE REMAINING ITEMS ON THE TEST ARE ABORTED AND THE NEXT TEST IS STARTED. KEEP THIS IN MIND WHILE INTERPRETING THE FOLLOWING ERROR DESCRIPTIONS.

UUT = UNIT UNDER TEST (99/4)
ADC = ANALOG TO DIGITAL CONVERTER (DIGITAL VOLTMETER)

STEP#	MESSAGE	FAILURE DESCIPTION
0	I/O RESET	PIN 3, I/O CONN., DID NOT START LOW AND THEN GO HIGH AT MOST 750 MS. AFTER APPLYING POWER TO THE UUT.
	SYSTEM VOLTAGE	A MEASURED VOLTAGE ON ONE OF THE CONNECTORS WAS OUT OF TOLERANCE. SEE THE ERROR TABLE FOR ACCEPTABLE LIMITS. THE ACTUAL VOLTAGE MEASURED IS CALCULATED BY DIVIDING THE MEASUREMENT BY 204.8 . EXAMPLE : IF THE TWO ERROR PARAMETERS ARE 2 AND 1100, THE I/O PORT`S +5 V ACTUALLY MEASURED 1100/204.8 = 5.37 V. ALSO, NOTE THAT AN `OPEN` (I.E. NO CONNECTION) WILL NOT NECESSARILY READ 0 VOLTS.

1	SYSTEM CLOCK	THE MEASURED FREQUENCY IS NOT WITHIN SPECS. SEE THE ERROR TABLE TO FIND WHICH CLOCK WAS INCORRECT AND FOR THE CORRECT TOLERANCES. THE ACTUAL FREQUENCY IS THE MEASURED VALUE X 100.
2	LOAD DATA	THE TEST SET TRIED TO GET THE UUT TO RUN THE TEST SOFTWARE BY PULLING PIN 13, I/O PORT, LOW. THE TEST SOFTWARE IS RUN FROM THE GROM PORT, WHILE THE RESULTS ARE SENT VIA THE I/O PORT. THUS, IF THIS TEST FAILS BUT THE `UUT WAIT STATE` TEST PASSES, THEN THE RESULTS WERE NOT RECEIVED. PROBABLE CAUSES OF THIS ARE : I/O PORT DATA BUS DRIVERS I/O PORT ADDR BUS DRIVERS I/O PORT BUS CONTROL DRIVERS (DBIN,WE, ETC) IF THE `UUT WAIT STATE` TEST ALSO FAILS, ANY OF THE FOLLOWING ITEMS COULD BE BAD IN ADDITION TO THE ABOVE : GROM PORT DATA LINES GROM PORT ADDRESSS LINES PIN 13, I/O PORT (LOAD) TMS 9900 AND SUPPORT CHIPS (99/4 DEAD)
3	UUT WAIT STATE	THE TEST SET LOOKS AT THE DURATION OF A MEMORY READ ON THE I/O PORT. IF THE `LOAD DATA` TEST FAILS, THIS TEST MAY FAIL AS A RESULT. OTHERWISE, THE SUSPECT H/W INCLUDE : I/O PORT ADDRESS AND BUS CONTROL LINES TIMING CONTROL OF UUT (U613 AND RELATED IC)
	*****	FROM THIS POINT ON, EITHER OF TWO ERRORS MAY OCCUR AT ANY TIME. BOTH OF THESE ERRORS WILL CAUSE POWER TO BE TURNED OFF TO THE UUT AND ALL REMAINING TEST TO BE ABORTED. THESE ERRORS ARE :
***	PROCESSORS OUT OF SYNC	IF THIS ERROR OCCURRED ON STEP 3, IT MAY BE DUE TO THE `LOAD DATA` TEST FAILING. IF NOT, THE PROBABLE BAD UUT H/W IS : I/O PORT PIN 22 (CRUCLK) I/O PORT ADDRESS BUS GROM PORT PIN 8 (A15/CRUOUT) IF THIS ERROR OCCURS AFTER STEP 3, THE UUT PROBABLY IS LOST OR EXECUTED TEST SOFTWARE BEFORE IT WAS TOLD TO. CAN BE DUE TO AC NOISE IN THE TEST SET OR THE UUT I/O PORT FAILED DURING TESTING.
***	TEST TIME OUT	THIS FAILURE INDICATES THE UUT TOOK TOO LONG TO ACKNOWLEDGE TO THE TEST SET AT THE END OF A TEST. PROBABLE CAUSES ARE THE UUT FAILING DURING TESTING OR AC LINE NOISE CAUSING A POWER GLITCH.
8	MC6810 RAM	THE UUT PERFORMED TWO SELF TESTS ON THE INTERNAL MCM6810 STATIC RAMS USING A CRC ALGORITHM. AN ERROR INDICATES ONE OR BOTH OF U608 AND U609 IS BAD.

4	I/O ADDR BUS	SIGNIFIES EITHER A SHORT OR AND OPEN ON THE ADDRESS LINES OF THE I/O PORT. ADDITIONALLY, PIN 26 OF THE I/O PORT MAY ALSO BE BAD (WE).
	GROM ADDR BUS	SAME AS I/O ADDR BUS BUT ON THE GROM PORT. THE OTHER POSSIBILITY IS PIN 32, GROM PORT (WE). IF THE I/O ADDRESS BUS FAILS FIRST, THE GROM ADDRESS BUS DOES NOT GET VERIFIED.
	I/O DATA BUS	A FAILURE INDICATES A SHORT OR AN OPEN ON THE DATA BUS OF THE I/O PORT. SUSPECT H/W INCLUDES : UUT DATA DRIVERS (LS244 AND LS374) UUT DATA BUS CONTROL I.C`S.
	GROM DATA BUS	SAME AS THE I/O DATA BUS ERROR BUT OCCURS ON THE GROM PORT. SINCE THE DATA LINES ARE IN PARALLEL IF THE I/O BUS PASSES, THE PROBLEM IS NOT THE BUS DRIVERS BUT IS MOST LIKELY AN `OPEN`.
5	INVALID DECODE	THIS TEST FAILED BECAUSE ONE OF THE DECODED ADDRESS LINES WAS ACTIVE WHEN IT SHOULDN`T HAVE BEEN. SUSPECTS ARE : I/O PORT PIN 9 DBIN I/O PORT PIN 32 MEMEN I/O PORT PIN 2 SBE I/O PORT PIN 28 MBE GROM PORT PIN 25 DBIN GROM PORT PIN 34 ROMG
	SBE BAD	I/O PORT PIN 2 DID NOT GO ACTIVE PROPERLY
	MBE BAD	I/O PORT PIN 28 DID NOT GO ACTIVE PROPERLY
	ROMG BAD	GROM PORT PIN 34 DID NOT GO ACTIVE PROPERLY
6	I/O ADDR BUS	THIS ERROR IS SIMILAR TO THE ONE IN STEP 4. IF THIS STEP FAILS BUT STEP 4 PASSED, THE PROBLEM IS MOST LIKELY PIN 22, I/O PORT. IF BOTH STEPS FAILED, THE ERROR IS WITH ONE OF THE I/O ADDRESS LINES ONLY.
	GROM ADDR BUS	SIMILAR TO ABOVE EXCEPT THE SUSPECT IS NOW PIN 4, GROM PORT, IF THIS STEP FAILED ALONE.
	CRU SINGLE BIT WRITE	THE UUT FAILED TO DO A `SBO` OR `SBZ` CORRECTLY. BAD HARDWARE MAY BE : I/O PORT PIN 19 A15/CRUOUT I/O PORT PIN 22 CRUCLK GROM PORT PIN 8 A15/CRUOUT GROM PORT PIN 4 CRUCLK I/O PORT ADDRESS BUS
	CRU MULTI-BIT	THE UUT FAILED A `LDCR` INSTRUCTION. IF THIS TEST FAILED AND THE SINGLE BIT WRITE PASSED, THE I/O ADDRESS BUS IS BAD OR THE TMS 9900 IS DEFECTIVE.
	CRU READ	THE UUT FAILED A `TB` INSTRUCTION. THE H/W IN QUESTION INCLUDES : I/O PORT PIN 33 CRUIN GROM PORT PIN 6 CRUIN I/O ADDRESS BUS

7	GROM DATA	THE UUT CONSOLE GROMS FAILED A BYTE-BY-BYTE DATA COMPARISON WITH THE SET OF GROMS IN THE TEST SET. IF THE ERROR ADDRESS IS >0000 - >17FF, GROM 2003 IS BAD. AN ADDRESS OF >2000 - >37FF MEANS GROM 2004 FAILED, AND FROM >4000 - >57FF MEANS GROM 2005 IS BAD.
	GROM READ ADDRESS ERROR	INDICATES ONE OF THE GROMS FAILED A READ ADDRESS TEST. THE ADDRESSES LISTED ABOVE INDICATE WHICH GROM IS BAD.
8	4732 ROM DATA	ONE OF THE TMS4732 ROMS FAILED A BYTE-BY-BYTE COMPARISON WITH A GOOD SET IN THE TEST SET. IF THE ERROR ADDRESS IS EVEN, U610 IS DEFECTIVE. IF THE ERROR ADDRESS IS ODD, U611 IS DEFECTIVE.
9	RAM TEST ERROR	THE 16K OF VDP RAM IS EXERCISED BY THE UUT WITH THE RESULTS PASSED ON TO THE TEST SET. BY COMPARING THE ACTUAL DATA WITH THE EXPECTED DATA IT CAN BE DETERMINED WHICH RAM CHIP(S) ARE BAD. THE MSB IS `D0` AND CORRESPONDS TO U109, WHILE THE LSB IS `D7` WHICH RELATES TO U102. SEE UUT SCHEMATIC FOR ALL OTHERS.
10	UUT HOLD	THE 99/4 IS PLACED IN A HOLD STATE AND THE TEST SET VERIFIES `HOLDA` IS GENERATED. UPON FAILURE, SUSPECT H/W INCLUDES : I/O PORT PIN 12 READY/HOLD I/O PORT PIN 41 HOLDA/IAQ
11	JOYSTICK DATA	THE JOYSTICK PORT WAS EXERCISED BY THE TEST SET AND AN ERROR WAS FOUND. THE ASSOCIATED TMS9901 OUTPUTS AND INPUTS OF THE UUT SHOULD BE CHECKED.
12	CASS. MOTOR	EACH MOTOR CONTROL (CS1 AND CS2) IS CHECKED FOR THE ABILITY TO SINK THE REQUIRED CURRENT. THE PARAMETER MEASURED IS THE VOLTAGE DROP THRU A 50 OHM RESISTOR PULLED TO 5 V. A VALUE HIGHER THAN EXPECTED USUALLY INDICATES A BAD TRANSISTOR/ OPTOISOLATOR. THE TABLE NUMBER OF THE PRINTOUT WILL INDICATE WHICH MOTOR CONTROL FAILED. AS BEFORE, THE ACTUAL VOLTAGE IS THE MEASURED VALUE DIVIDED BY 204.8 .
13	CASS. OUTPUT	A BIT STREAM IS SENT OUT THE CASSETTE MAG OUT TERMINAL AND VERIFIED, USING THE TEST SET ADC, FOR PROPER AMPLITUDE. THESE VALUES ARE RELATIVE AND CANNOT BE CORRELATED TO AN ACTUAL VOLTAGE. A FAILURE USUALLY INDICATES A DEFECTIVE CASSETTE OUTPUT CIRCUITRY.
14	CASS. INPUT	A BIT SREAM IS GENERATED IN THE TEST SET AND SENT TO THE MAG IN PIN OF THE CASETTE PORT. A FAILURE HERE POINTS TO A BAD CASSETTE INPUT CIRCUIT.

15	AUDIO GATE	A CASSETTE INPUT IS GENERATED AS ABOVE AND THE AUDIO GATE IS TURNED ON AND OFF TO VERIFY CORRECT OPERATION. A FAILURE ON THIS TEST ALONG WITH TEST 14 PROBABLY MEANS THE SIGNAL WAS NOT GETTING TO TRANSISTOR Q405. A FAILURE OF THIS TEST ALONE INDICATES Q405 OR ITS COMPANION COMPONENTS MAY BE DEFECTIVE OR THE SOUND CHIP (U511) IS BAD. THE MEASURED PARAMETER IS THE FREQUENCY OF THE INPUT SIGNAL AND SHOULD BE 300 HZ.
16	GROM RESET	THE RESET LINE ON THE GROM PORT WAS PULLED TO -5 V AND THE UUT SHOULD HAVE RESET. AN ERROR MEANS A FAILURE IN THE CIRCUITRY ASSOCIATED WITH PIN 1 OF THE GROM CONNECTOR. ALSO, A FAILURE ON THIS TEST MAY CASE THE REMAINDER OF THE TESTS TO FAIL, SINCE THE UUT WOULD NOT BE RUNNING THE GPL TEST SOFTWARE. PIN 21 OF THE GROM CONNECTOR MAY ALSO CAUSE THIS ERROR.
17	I/O INTERRUPT	THE UUT DID NOT ACKNOWLEDGE A TEST SET GENERATED INTERRUPT. SUSPECT H/W INCLUDES : I/O PORT PIN 4 EXT INT TMS 9901 U300
18	9919 TONE BAD	THE UUT EXECUTES GPL SOFTWARE TO EXERCISE THE TMS 9919 SOUND CHIP. THIS TEST CHECKS A LOW AND HIGH FREQUENCY ON EACH TONE REGISTER, USING THE TEST SET'S FREQ. COUNTER. AN ERROR MAY BE CAUSED BY A DEFECTIVE SOUND CHIP, OR AN OPEN ON EITHER THE EARPHONE CONNECTOR OR THE VIDEO CONNECTOR. A FAILURE HERE WILL CAUSE THE REST OF THE SOUND TESTS TO BE SKIPPED.
19-25	TONE ATTEN.	THE UUT RUNS THRU A SERIES OF ATTENUATION TESTS WITH THE 9919 TONE REGISTERS. THESE VALUES ARE MEASURED USING THE TEST SET ADC, BUT THE VALUES ARE RELATIVE ONLY AND CANNOT BE STATED AS AN ABSOLUTE VOLTAGE. A FAILURE ON THIS TEST ALONE MAY NOT NECESSARILY MEAN A BAD SOUND CHIP, DEPENDING ON THE DEVIATION FROM THE ALLOWED VALUES.
26	NOISE ATTEN.	THE SAME AS THE PREVIOUS TEST BUT RUN ON THE TWO NOISE REGISTERS IN THE SOUND CHIP. USE THE SAME DISCRETION AS EXPLAINED ABOVE IN FAILING A UNIT BASED ON A FAILURE HERE ONLY.
27	EXTERNAL AUDIO	THE TEST SET GENERATES A 1200 HZ TONE AND APPLIES IT TO THE TWO AUDIO INPUTS. A FAILURE HERE, ALONG WITH A FAILURE OF THE AUDIO GATE, USUALLY INDICATES A BAD TMS9919 (U511). IF THE CASSETTE PORT INPUT FAILS BUT THE I/O PORT INPUT PASSES, THEN THE ERROR IS IN THE CASS. AUDIO CIRCUITRY. THE TWO INPUTS ARE : I/O PORT PIN 44 SOUND IN CASS. PORT PIN 4 CASS. AUDIO IN THE OUTPUT IS VERIFIED BY THE TEST SET'S FREQ COUNTER LOOKING AT THE EARPHONE CONNECTOR.

28	AUDIO SUMMING	THE UUT TURNS ON SUCCESSIVE TONE REGISTERS AND THE TEST SET VERIFIES THE SOUND AMPLITUDE OUT OF THE SOUND CHIP USING THE ADC. THE VALUES MEASURED ARE RELATIVE VOLTAGES ONLY AND ARE NOT TO BE RELATED TO AN ABSOLUTE LEVEL. A FAILURE HERE MEANS THE SOUND CHIP (U511) IS FAULTY OR THE EARPHONE CONNECTION IS NOT FUNC-TIONING.
***	OTHER ERRORS	THERE ARE THREE ADDITIONAL ERRORS THAT MAY OCCUR DURING THE TESTING CYCLE. ONLY ONE, THE `ABORT`, MAY INDICATE A UUT FAILURE. THESE THREE ARE :
	* ABORT *	THIS MEANS THE OPERATOR ABORTED TESTING WHILE THE TEST CYCLE WAS STILL IN PROGRESS. THERE SHOULD BE A NOTE FROM THE OPERATOR EXPLAINING THE REASON FOR THIS ACTION.
	TESTER GROMS	WHEN THIS MESSAGE APPEARS, DURING THE GROM BYTE-BY-BYTE COMPARISON TEST (STEP #7) THE INTERNAL REFERENCE GROMS IN THE TEST SET FAILED TO PERFORM CORRECTLY. R & M SHOULD BE NOTIFIED WHEN THIS ERROR OCCURS.
	UUT NOISE HIGH	EVERY TIME THE TEST SET PERFORMS A LEVEL CHECK ON THE EARPHONE OR THE CASSETTE MAO OUT PORT, AN ADDITION CHECK IS MADE ON THE NOIS LEVEL AT THESE CONNECTORS. THIS MESSAGE INDICATES THE MEASURED VALUE IS OUT OF TOLERANCE, WHICH MAY MEAN THE TEST SET NEEDS TO BE RECALIBRATED. REPORT THE OCCURANCE TO R & M.

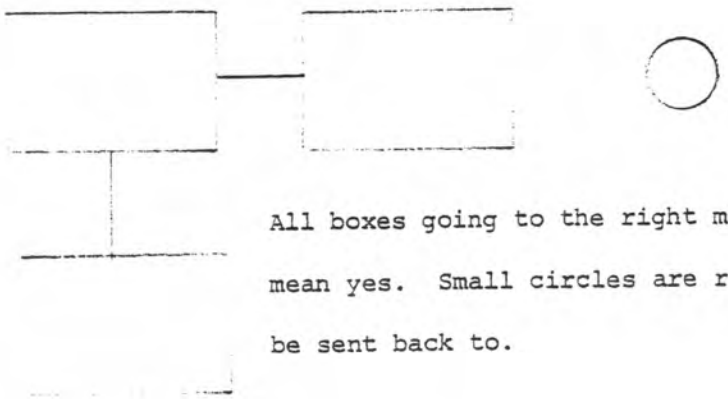
TEXAS INSTRUMENTS HOME COMPUTER

TROUBLE SHOOTING GUIDE

This guide will take you by the problem not neccessarly to the problem. You still need your basic troubleshooting skills. This guide is aimed at the new technician but still can be referenced when in doubt. Any questioned concerning this guide or Home Computer problems contact:

Curt Larsen ext 2449

Paul Greenwood ext 2771



All boxes going to the right mean no, all boxes going down mean yes. Small circles are reference points which you may be sent back to.

Front Panel Come Up? — NO → Check +5,-5, +12 At Power Supply — NO → Disconnect Supply, Check Voltages — NO → Power Supply TS&R

Front Panel Come Up? — YES

Check +5,-5, +12 At Power Supply — YES

Disconnect Supply, Check Voltages — YES → Find Shorts On Logic Board. Start Over

Front Panel Correct? — NO → Page 10

Front Panel Correct? — YES

CC

Respond To Any Key — NO → Page 10

Respond To Any Key — YES

Check 9900 Pins 8,9,28,25 for Clocks. Also U613-P11 U607-P11 U607-P3, U300-P11 For TTL Clocks — NO → Check U601 Pins 6,7,8,9,11,12,14+15 — NO → Check U601 For Voltage Pins 13=12v 20=5v — NO → Trace Etch To Problem

Check U601 Pins 6,7,8,9,11,12,14+15 — YES → Check Etches To Various Pins for Continuity

Check U601 For Voltage Pins 13=12v 20=5v — YES → Check Pin 5 for +5 — NO → Check R605, R606, C606 for Shorts

Check Pin 5 for +5 — YES → Check Tank Circuit, C603 L602, Y600 — NO → Change Defective Component

Check Tank Circuit, C603 L602, Y600 — YES → Probability U601

Plug in Diagnostic Prom

Plug in Diagnostic Prom — YES

Check 9900 Pins 8,9,28,25 for Clocks. Also U613-P11 U607-P11 U607-P3, U300-P11 For TTL Clocks — YES

Check Pin 38 U100 for Clock If Present Adj to 3.579545 — NO → Page 2

Check Pin 38 U100 for Clock If Present Adj to 3.579545 — YES → Page 3

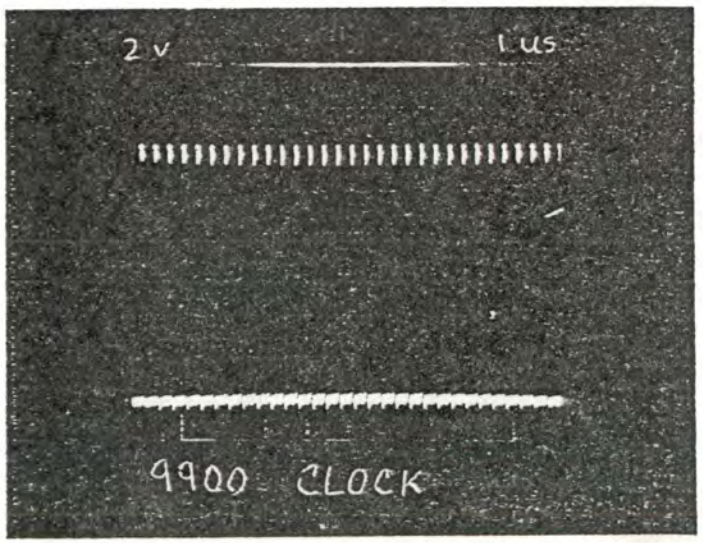
Read + Write Cassette — NO → Page 11

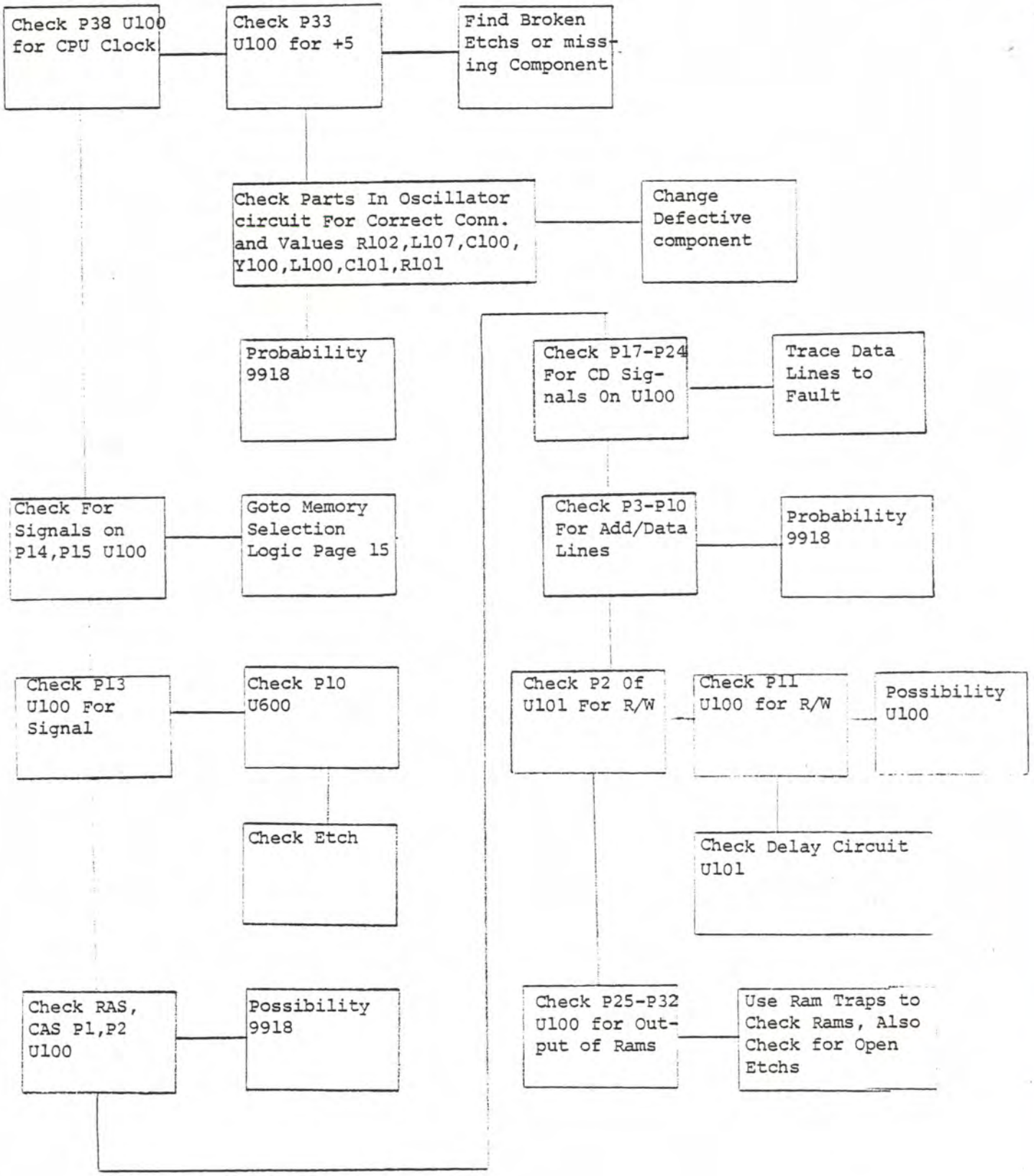
Read + Write Cassette — YES

Joysticks Operate? — NO → Page 12

Joysticks Operate? — YES

CC




Check P38 U100 for CPU Clock
Check P33 U100 for +5
Find Broken Etchs or missing Component
Check Parts In Oscillator circuit For Correct Conn. and Values R102,L107,C100, Y100,L100,C101,R101
Change Defective component
Probability 9918
Check P17-P24 For CD Signals On U100
Trace Data Lines to Fault
Check For Signals on P14,P15 U100
Goto Memory Selection Logic Page 15
Check P3-P10 For Add/Data Lines
Probability 9918
Check P13 U100 For Signal
Check P10 U600
Check P2 Of U101 For R/W
Check P11 U100 for R/W
Possibility U100
Check Etch
Check Delay Circuit U101
Check RAS, CAS P1,P2 U100
Possibility 9918
Check P25-P32 U100 for Output of Rams
Use Ram Traps to Check Rams, Also Check for Open Etchs

From Page 1

Page 3

Check P62 9900 For Correct Ready Signal

AA

Page 8

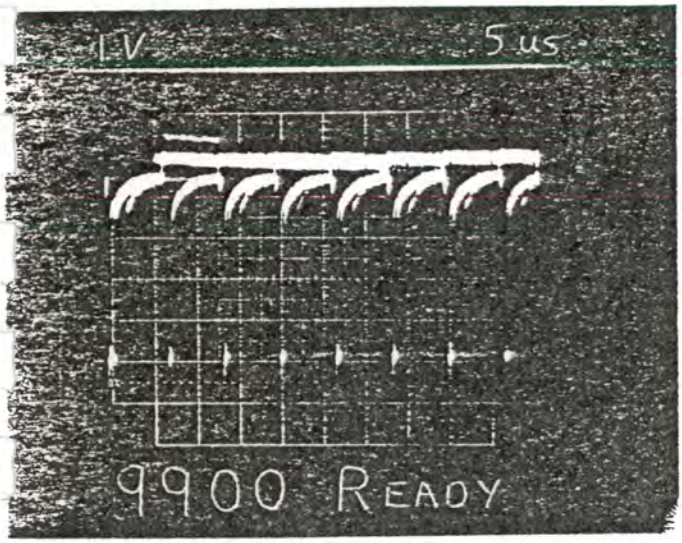
Check Reset P6 9900 for High Level

Check P5 U601 for High Level

Check R605, R606, C606

Check for Signal P5 U601, P6 9900

Probability U601



Page 4

Pull Groms, Sound Chip Check Ready Good?

Check P12 U607 for High Level

Check P3 U506 for High Level

JJ

Page 5

Check Etch P3 U506, P12 U607

Replace Groms One at a Time Check Ready Each Good?

First Grom Good

Goto Grom Check Page 9

Possibility Bad Groms, Sockets, Etchs

Replace Sound Chip and Check Ready Good?

Check for Supply P8,p16 9919

Find Broken Etch or Buss Bar

Goto AA

Check for Clock P14

Check P38 VDP for Clock

Goto VDP Check Page 2

Possibility Sound Chip or Broken etch

Check Coax Between VDP and Sound Chip

From Page 3

Check P1 U506 for Low Level

Check P2 U508 for Low Level

Check P1 U508 for High Level

Check R504 for +5 at Both Ends

Find Open Etch to +5 or short on signal side of U504

Check Etch U508, U506

Check Etch R504, U508

Check P7,P14 for Voltage

Find Problem

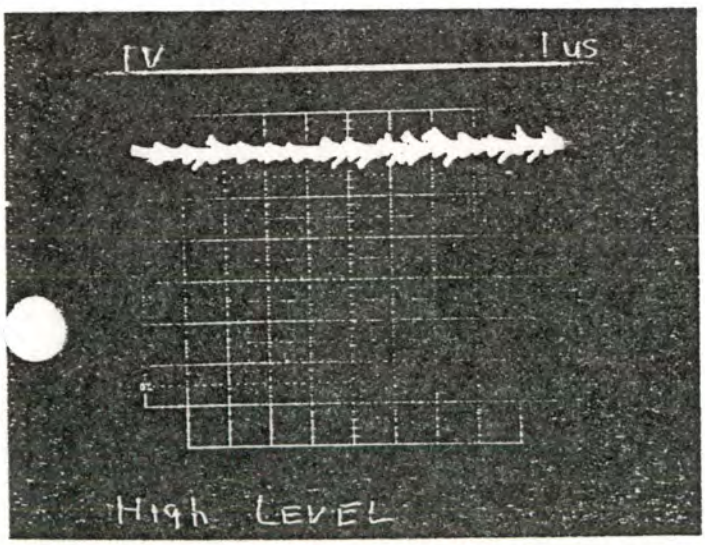
Check P7, P14 for Voltage

Find Problem

Probability U506

Probability U508

JJ



From 3

Check [illegible] U607 for High Level

Check P10,13, 14 for +5

Find Broken Etch

DD

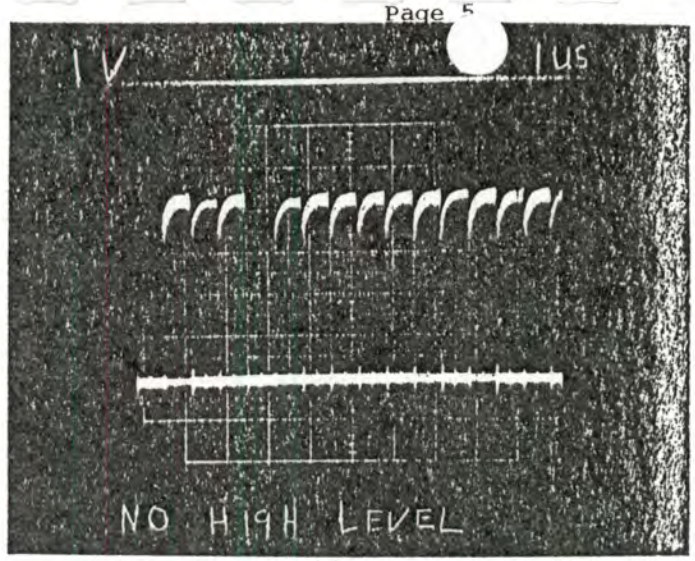
Check P11 U607 for Clock

Check P15 U601 for Clock

Goto CC Page 1

Probability U607

Find Broken Etch Between P15 U601 and P11 U607



Check P9 U613 for High Level

Check for Broken Etch Between P9 U607 and P9 U613

Check P10 U613 for Active Signal

Check P11 U605 for Signal

Check P12 U605 for Signal

Check P3 U605 for Signal

Check P2 U605 for Signal

Check P63 9900 for Signal

Possibility if All Voltages, Clocks, Reset, Load, Intreq are Present or Accounted for, Bad 9900

DD

Find Broken Etch

Check P13 U605 for No High Level

Find Broken Etch

Goto DD

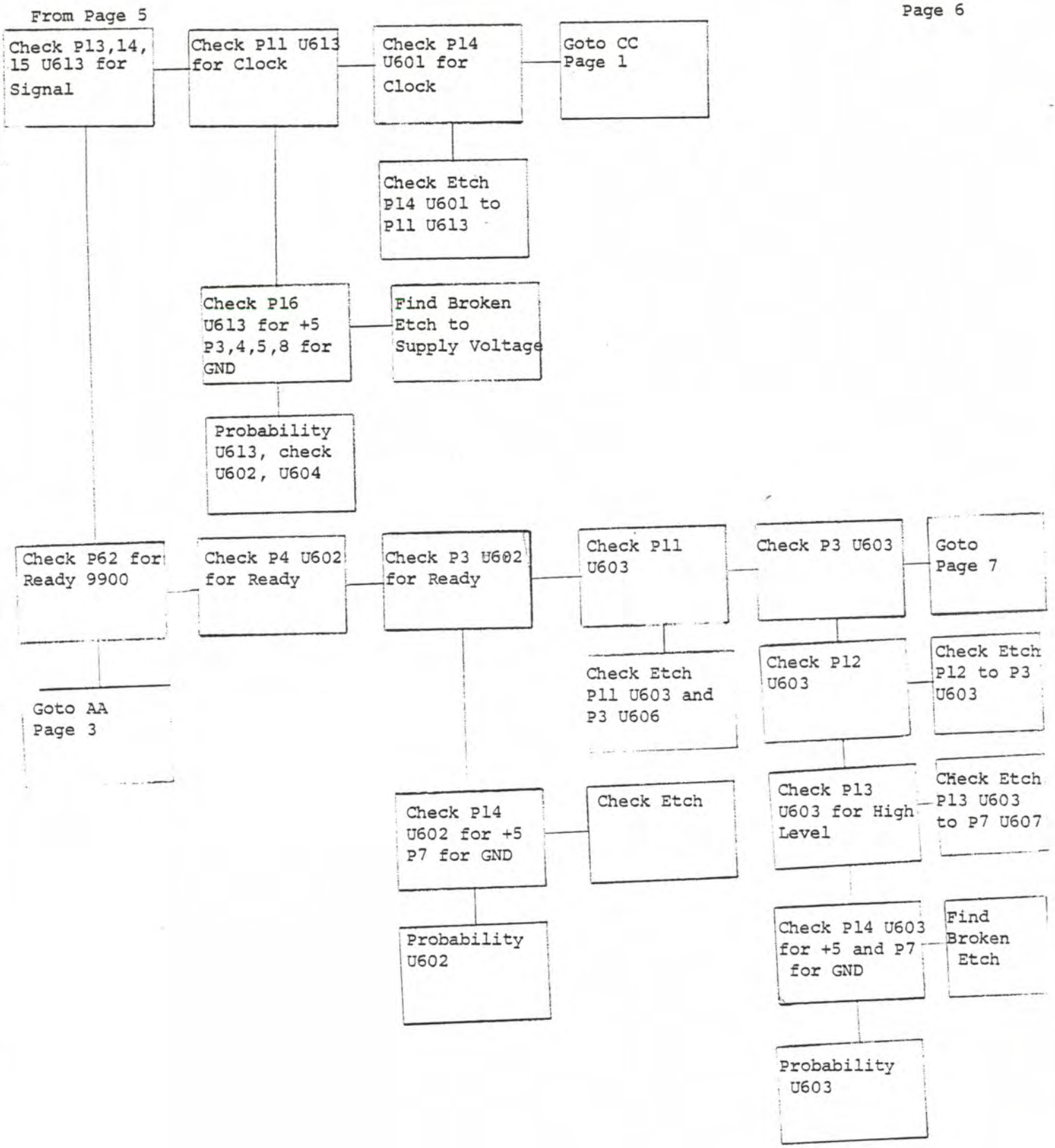
Find Broken Etch

Page 6

Check P14 U605 for +5

Find Broken Etch

Possibility U605


From Page 5
Check P13,14, 15 U613 for Signal
Check P11 U613 for Clock
Check P14 U601 for Clock
Goto CC Page 1
Check Etch P14 U601 to P11 U613
Check P16 U613 for +5 P3,4,5,8 for GND
Find Broken Etch to Supply Voltage
Probability U613, check U602, U604
Check P62 for Ready 9900
Check P4 U602 for Ready
Check P3 U602 for Ready
Check P11 U603
Check P3 U603
Goto Page 7
Goto AA Page 3
Check Etch P11 U603 and P3 U606
Check P12 U603
Check Etch P12 to P3 U603
Check P14 U602 for +5 P7 for GND
Check Etch
Check P13 U603 for High Level
Check Etch P13 U603 to P7 U607
Probability U602
Check P14 U603 for +5 and P7 for GND
Find Broken Etch
Probability U603

From Page 6

Check P1,2 U603 for Active Signal

P1

Check P6 U612 for Signal

Check P4,5 U612 for Signal

P4

Check P3 U612 for Signal

Check P2 U612 for Signal and P1 for +5

Check Etch to +5

P2

P5

Check Etch P6 U612 to P1 U603

Check P14,7 U612 for Voltage if Yes Prob. U612

Check Etch

Goto EE

Check Etch P15 U613 to P2 to 612

EE

Check P14,7 for Correct Voltages

Check Etch

Check Etch P5 U612 to P13 U613

Probability U603

Check P2 U604

Check Etch P2 U604 to P2 U603

Check P1 U604

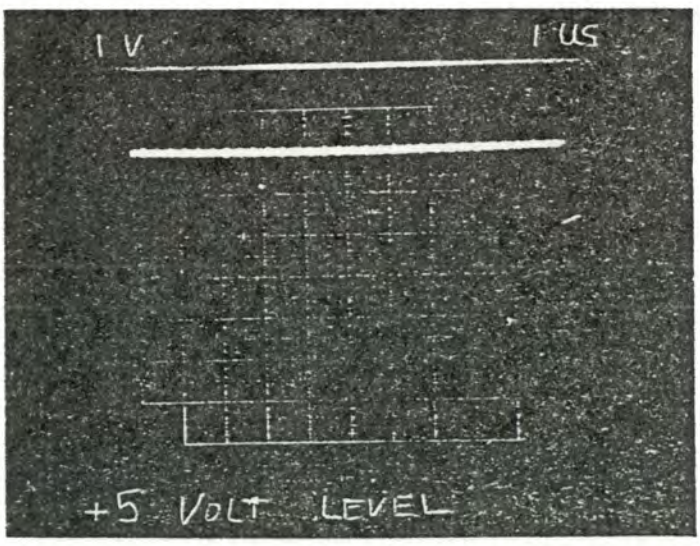
Check Etch P1 U604 to P11 U605

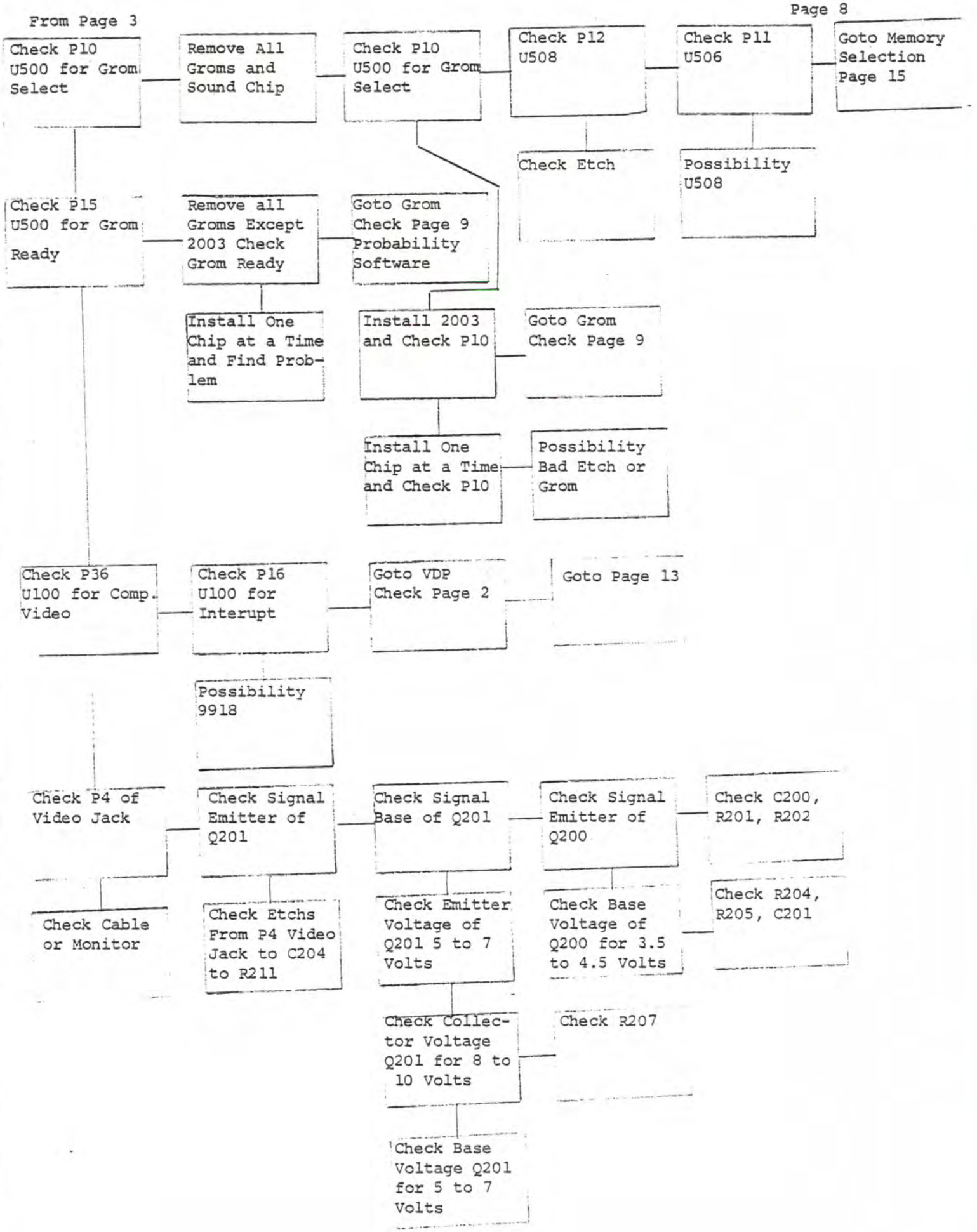
Check P14,7 U604 for Correct Voltages

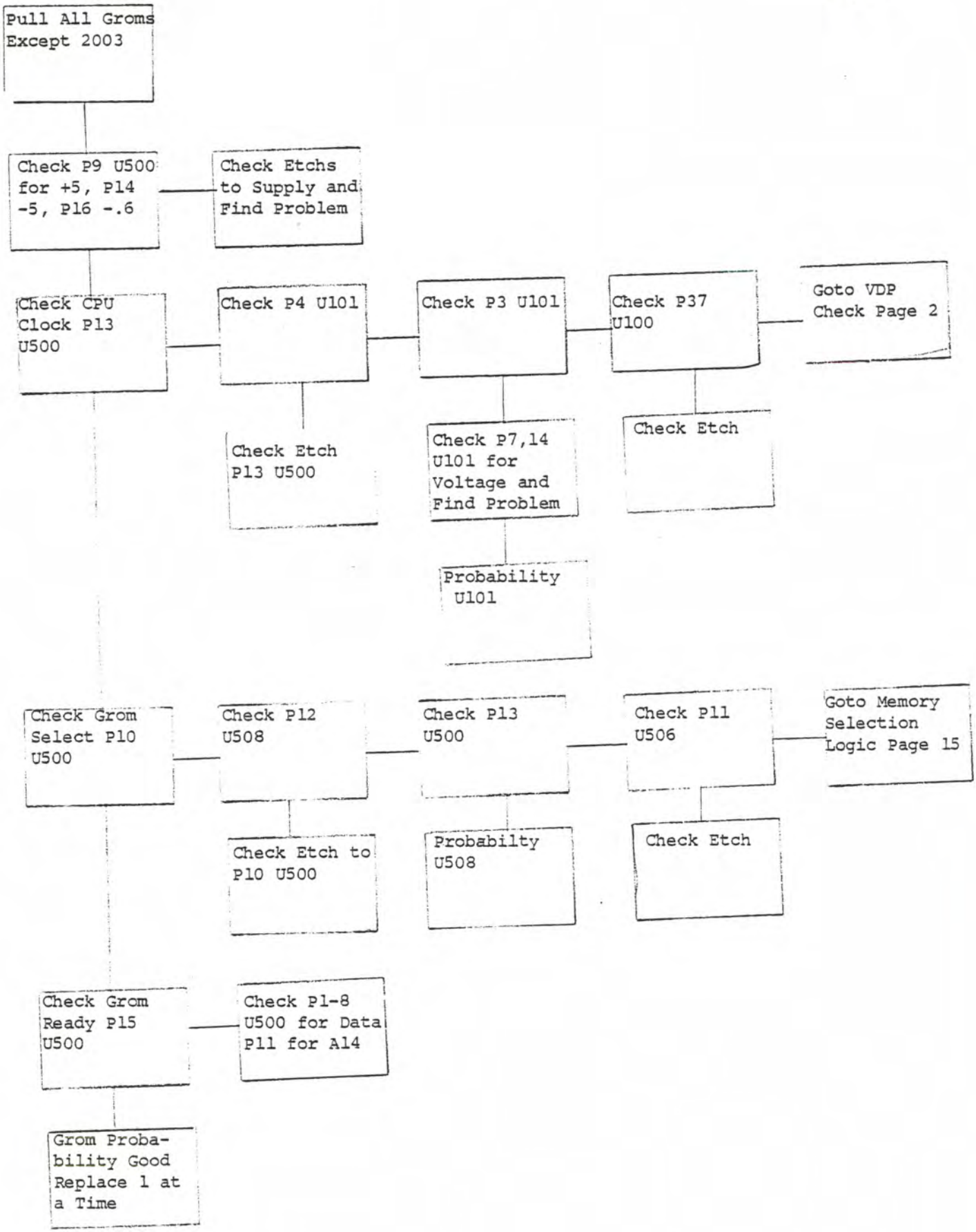
Check Etchs

EE

Probability U604




From Page 3
Check P10 U500 for Grom Select
Remove All Groms and Sound Chip
Check P10 U500 for Grom Select
Check P12 U508
Check P11 U506
Goto Memory Selection Page 15
Check Etch
Possibility U508
Check P15 U500 for Grom Ready
Remove all Groms Except 2003 Check Grom Ready
Goto Grom Check Page 9 Probability Software
Install One Chip at a Time and Find Problem
Install 2003 and Check P10
Goto Grom Check Page 9
Install One Chip at a Time and Check P10
Possibility Bad Etch or Grom
Check P36 U100 for Comp. Video
Check P16 U100 for Interupt
Goto VDP Check Page 2
Goto Page 13
Possibility 9918
Check P4 of Video Jack
Check Signal Emitter of Q201
Check Signal Base of Q201
Check Signal Emitter of Q200
Check C200, R201, R202
Check Cable or Monitor
Check Etchs From P4 Video Jack to C204 to R211
Check Emitter Voltage of Q201 5 to 7 Volts
Check Base Voltage of Q200 for 3.5 to 4.5 Volts
Check R204, R205, C201
Check Collector Voltage Q201 for 8 to 10 Volts
Check R207
Check Base Voltage Q201 for 5 to 7 Volts


Pull All Groms Except 2003
Check P9 U500 for +5, P14 -5, P16 -.6
Check Etchs to Supply and Find Problem
Check CPU Clock P13 U500
Check P4 U101
Check P3 U101
Check P37 U100
Goto VDP Check Page 2
Check Etch P13 U500
Check P7,14 U101 for Voltage and Find Problem
Check Etch
Probability U101
Check Grom Select P10 U500
Check P12 U508
Check P13 U500
Check P11 U506
Goto Memory Selection Logic Page 15
Check Etch to P10 U500
Probabilty U508
Check Etch
Check Grom Ready P15 U500
Check P1-8 U500 for Data P11 for A14
Grom Proba-bility Good Replace 1 at a Time

Use Ram Trap to Locate Faulty Ram. Good?

Change Ram Found by Ram Trap

Possibility In 4732's and Groms

Use Ram Trap to Test Groms Good?

Change Defective Grom

Change 1 Rom at a Time to Locate Fault

MM

Check Keyboard P1,3,5,7,9, 10,12,14,16, 18 for Signal

Check P7,9,10, 11,12 U302 for Signals

Check P1,3, 13,15 U302 forSignals

Check P21,22, 26 U300 for Signal

Check P40,1: U300 for +5 P16 for Gnd P10 for Clock Check All Necessary Pins to Insure Chip is Functional Address Lines CPU Lines Possibility 9901, 4732's for Software

Check R301- R309 and Etchs to Keyboard

Check P2,8, 14 U302 for Gnd P16 for +5 Poss. U302

Check For Broken Etch

Check for Signal On P2,4, 6,8,11,13,15, 17 Upon Key Closure

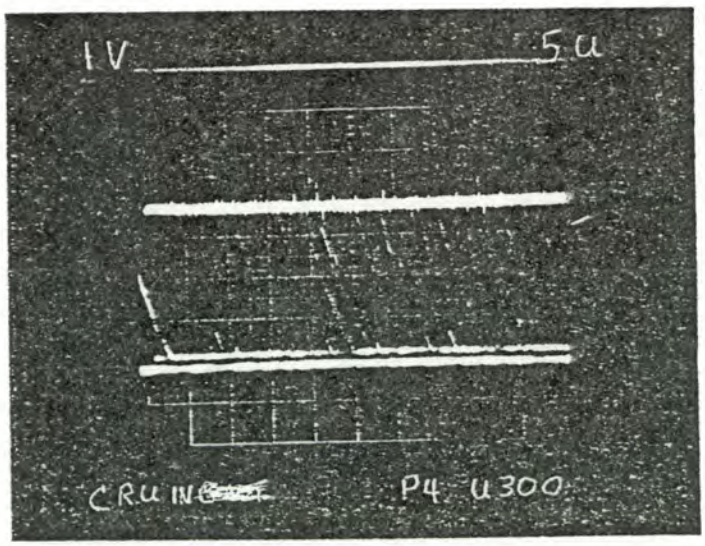
Possibility Keyboard

MM

Check P6,7,8, 9,31,32,33,34 U300 for Signal From Keyboard

Find Broken Etch

Goto MM



From Page 1

Will Not Write Cassette

Check P5 of Cassette Jack for Correct Signal

Check P28 of 9901 for Correct Signal

Insure H.C. is in Record Mode

Possibility Cassette is Not Reading

Check Write Circuit R400, R401,R402,C400 C408,C412

Will Not Read Cassette

Check If Read Signal is Present at R406

Check Cassette Cable, Check R404,R406,R409,C402 for Shorts

Check If Read Signal is Present P7 U400

Check R408,R410,C409,C411 for Shorts, Check P8 U400 for +5 P4 for -5

Check if Read is Present on P30 U300

Check CR402,R411,C412, R413,C413,C414 for Shorts

Check Amount of Jitter During Read Signal

Cassette Remote Control High Level

Check P23,19 U300 for High Level

Probabilty 9901

Check +5 on Collector Q402,Q404

Check for Broken Etch

Check for About 4 Volts On Emitter of Q402,Q404

If Emitter Has Low Voltage Replace Transistor

Check for Low Resistance Emitter to Collector Q401,3

Check Open Coupler and Transistor

Check C403 - C406 for Shorts

From Page 1

Check P5,6 U302 for Neg. Pulse

Insure Unit is Set Up for Joystick Program

Check P1,3, 13,15 U302 for Positive Pulses

Check P2,8, 14 U302 for Gnd P16 for +5 Poss. U302

Check P21,22, 26 U300 for Signal

Check for Broken Etchs

Check P40,1 U300 for +5, P16 for Gnd P10 for Clock, Check all Neccessary Pins to Insure Chip is Functional Address Lines, CPU Lines Possibility 9901, 4732's for Software

Move Joystick Position Check Input Pins on 9901 P6,7,8,9

Check Signal at Joystick Port Input & Output

Check Etchs to Port Both Input & Output

Input but No Output Bad Joysticks

Insure Capacitors C307-C310 and C317-C321 for Correct Value, Timing Critical, Other Possibilies, 4732's 9901, 74LS156

TT

Check P5 for DING

Check P6 U603

Check P5 U603 for Signal

Goto JJ Page 4

TT

Check Etchs

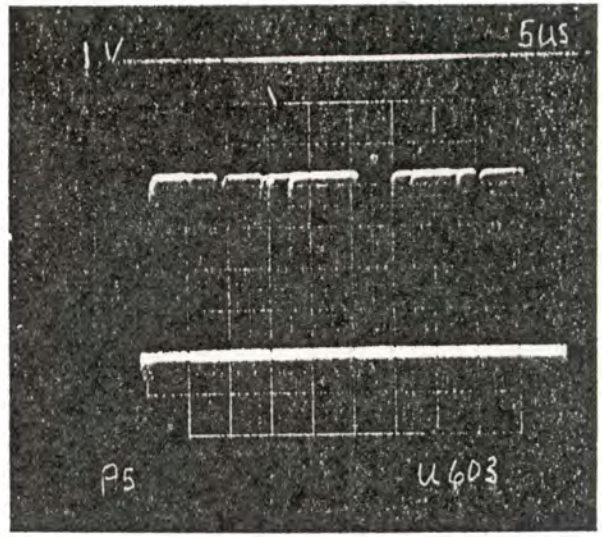
Check P4 U603 for DBIN

Check P10 U606 for DBIN

Goto DBIN Check Page 14

Probability U603

Check Etch



Check P1,19 U616 for DOG Signal

Check P8 U603

Check P9 U603

Goto DBIN Check Page 14

SS

RR

Check Etchs

Check P10 U603

Check P8 U602

Check P9 U602

Check P13 U613

Goto JJ Page 3

Check P11 U615

Goto RR

Possibility U603

Check Etchs

Possibility U602

Check Etchs

Check P19 U614 for DIOG

Check Pin 6 U606

Check P5 U606

Goto TT

Check P4 U606

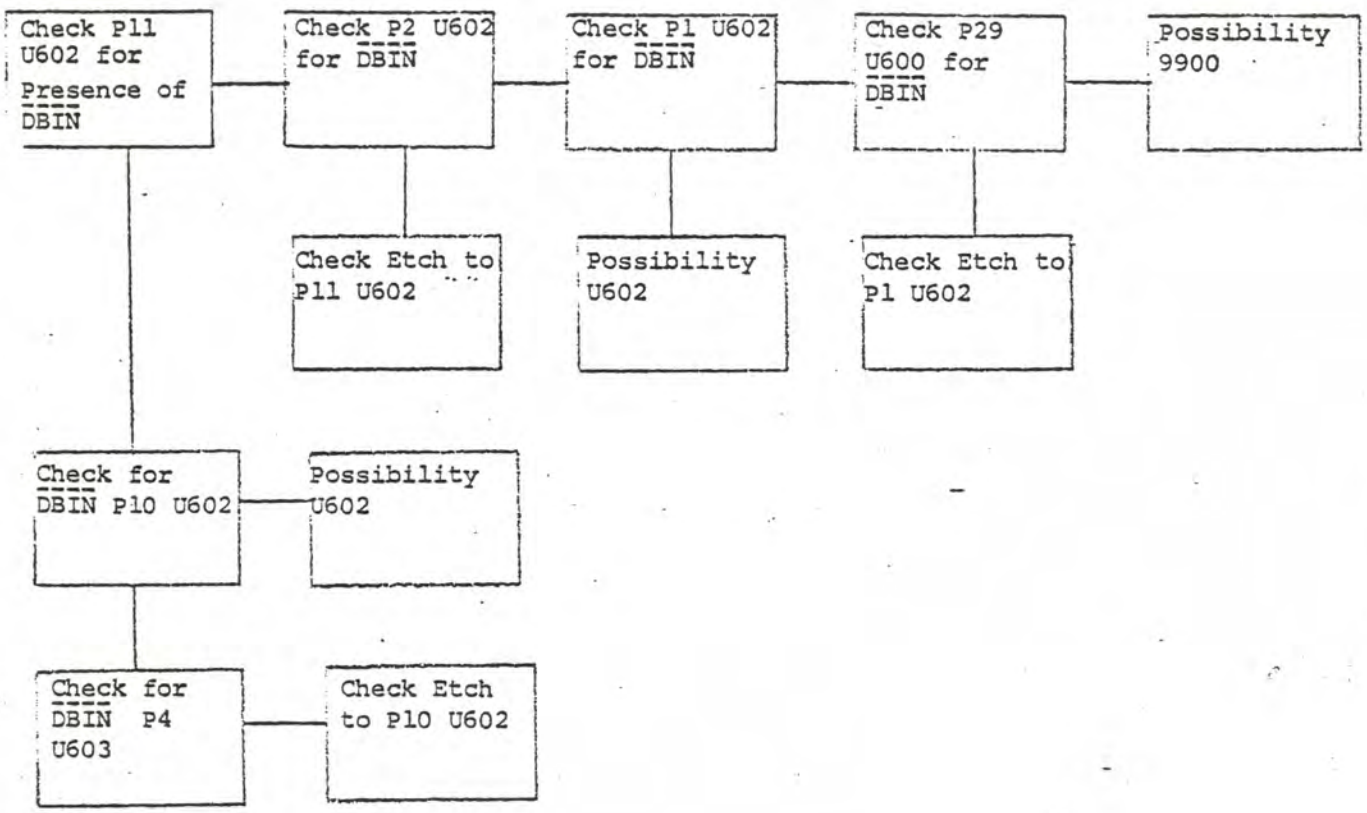
Goto SS

SS

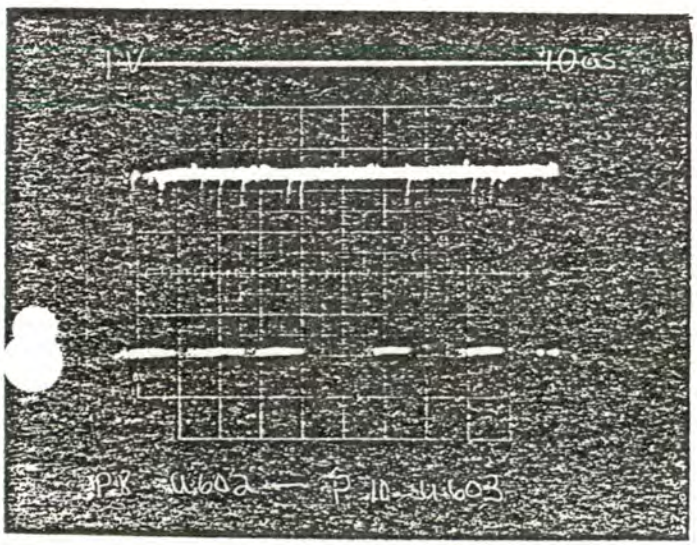
Pictures On Page 14

RR

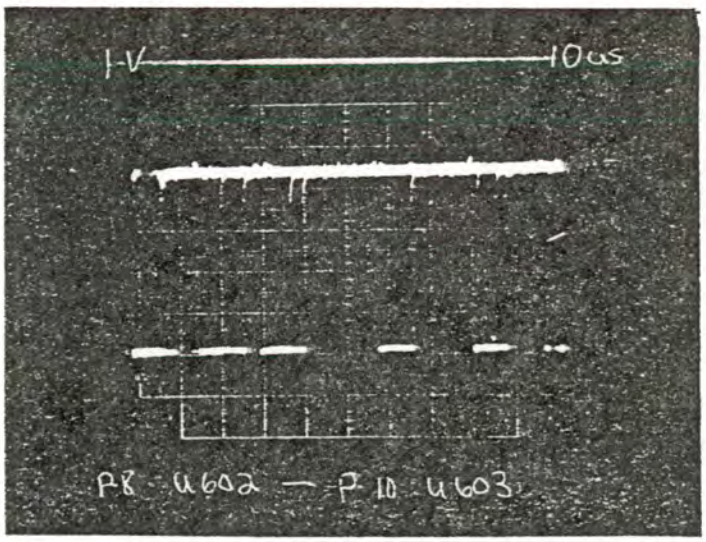
From Page 13



RR



SS



From Page 8,9

Remove All Groms and Sound Chip for Following Chips

Check P1,2,3 U504 for P1,2 Low P3 Active

Check P22,23, 24 9900 for Signal

Check Etchs

Check Memen P4 U504

Check P3 U605

Check P2 U605

Check P63 U600

Possibility 9900

Check Etchs

Possibility U605

Check Etchs

Check U504 Outputs P11, 15 Active P7-15

Check P6,16 U504 for +5 Pins 5,8 for GND

Check Etchs to Power Supply

Possibility 9900 Sending Bad Address or U504 Bad

Check for 9900 Signals INTREQ CRUIN Address Lines

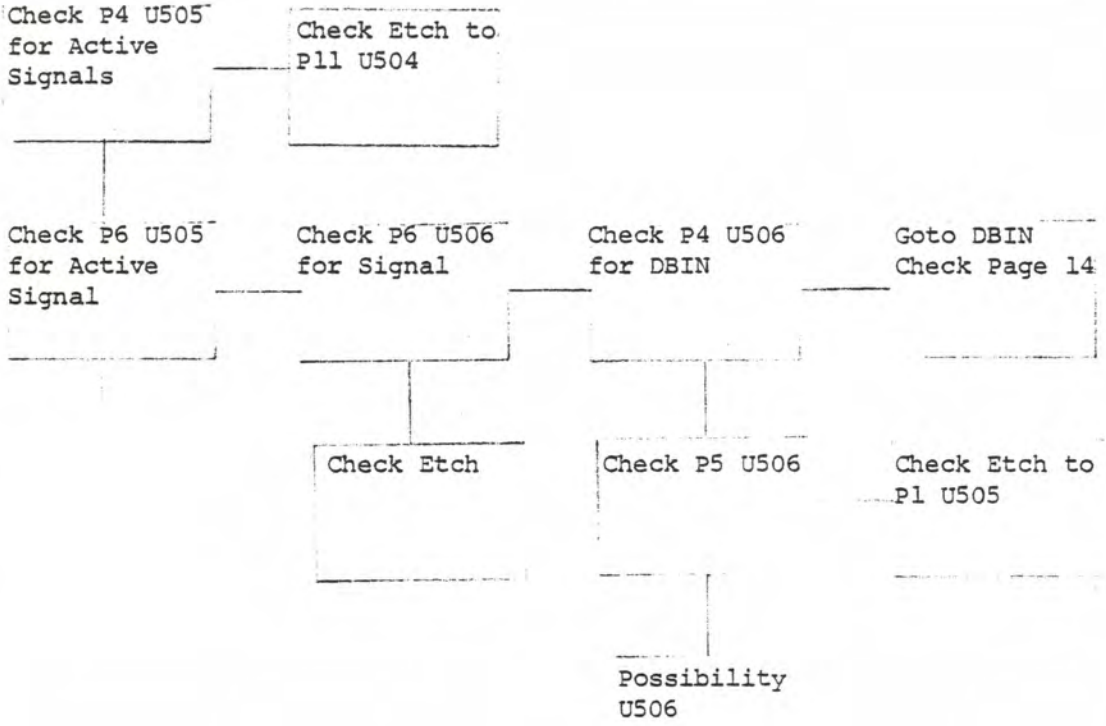
Goto Page 17

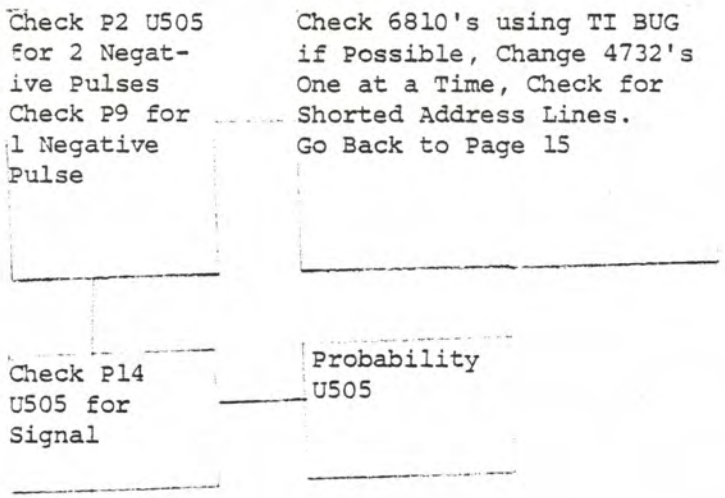
Check P1,2,3, 5 U505 for Address Lines

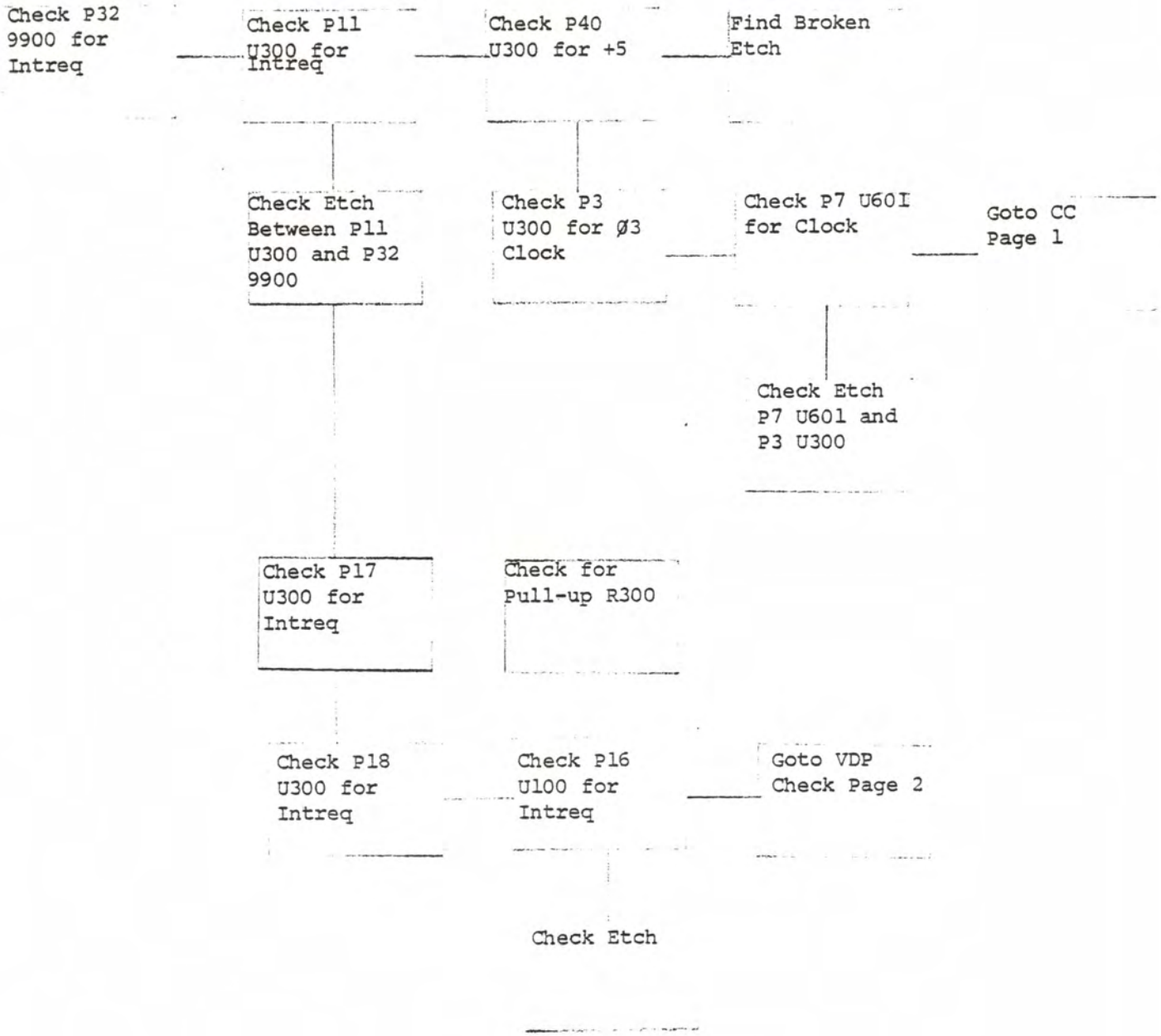
Check P19,20, 21 9900 for Signals

Check Etchs

Goto Page 16


Check P4 U505 for Active Signals
Check Etch to P11 U504
Check P6 U505 for Active Signal
Check P6 U506 for Signal
Check P4 U506 for DBIN
Goto DBIN Check Page 14
Check Etch
Check P5 U506
Check Etch to P1 U505
Possibility U506


Check P2 U505 for 2 Negative Pulses Check P9 for 1 Negative Pulse
Check 6810's using TI BUG if Possible, Change 4732's One at a Time, Check for Shorted Address Lines. Go Back to Page 15
Check P14 U505 for Signal
Probability U505
Memory Selection Good


Check P32 9900 for Intreq
Check P11 U300 for Intreq
Check P40 U300 for +5
Find Broken Etch
Check Etch Between P11 U300 and P32 9900
Check P3 U300 for Ø3 Clock
Check P7 U60I for Clock
Goto CC Page 1
Check Etch P7 U601 and P3 U300
Check P17 U300 for Intreq
Check for Pull-up R300
Check P18 U300 for Intreq
Check P16 U100 for Intreq
Goto VDP Check Page 2
Check Etch

TEST PROCEDURE BEGINS FROM COLD START

A → ATTACH VIDEO CABLE
TURN ON POWER

FRONT PANEL UP.? YES → RESPOND TO ANY KEY YES → SELECT KEY "ONE" → GO TO BASIC TEST PROGRAM

RESPOND TO ANY KEY NO → GO TO 9901 TEST → TO C

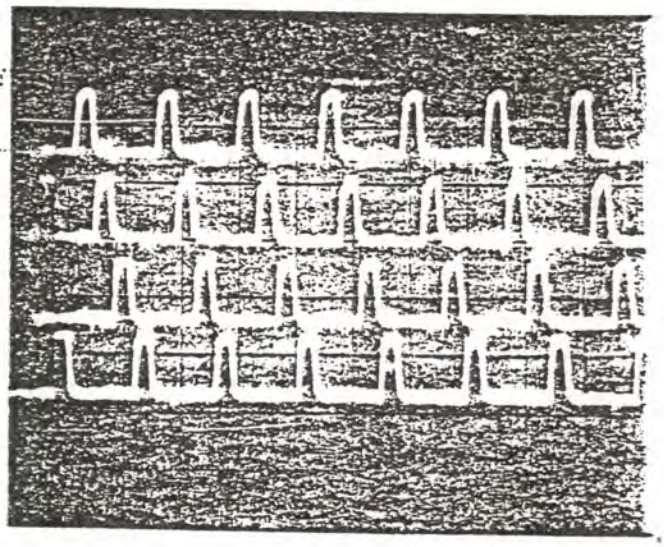
FRONT PANEL UP.? NO

1. CHECK +5, -5, +12 AT POWER SUPPLY
2. CHECK SAME AT INTERCONNECT TO CPU BOARD

SUPPLY GOOD? NO → DISCONNECT SUPPLY AND REPEAT TEST

SUPPLY GOOD? YES

1. CHECK LS 362 PINS 8, 9, 11, AND 12. SEE DIAGRAM RIGHT
2. CHECK LS 362 PINS 14, 15, 7, AND 6



12 VOLT 4 PHASE CLOCKS

SUPPLY GOOD? NO → POWER SUPPLY R+L → D

SUPPLY GOOD? YES

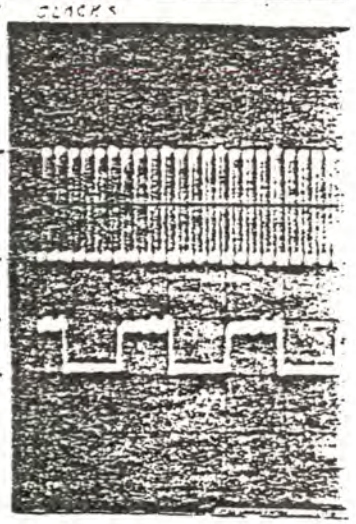
OK IN AREA OF 4027's FIRST

CHECK M.B. 1 AND 2 SUPPLY FOR SHORTS TO GND → TO REPAIR SHORTS → A

Φ CLOCKS GOOD? NO → LS 362 TESTS → E

REQUIRES FREQUENCY METER

M → 1. 9918 PIN 38 - 3.579545 MHz ± 100Hz ADJUST AS NEED AT CRYSTAL.
2. 9918 PIN 37 - 447KHz DIAGRAM RIGHT



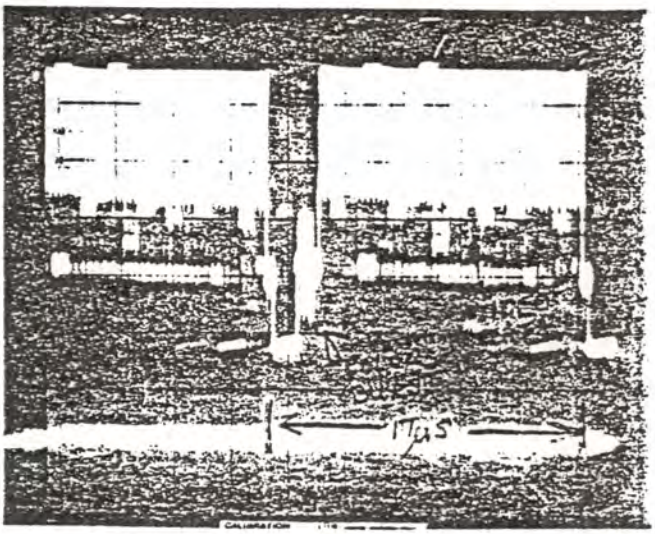
VDP CLOCKS GOOD? NO → VDP CLOCK TESTS → F

AT THIS TIME SYSTEM SUPPLIES AND CLOCKS SHOULD BE GOOD; 90% OF SYSTEM PROBLEMS HAVE BEEN ELIMINATED - NEXT TEST SYSTEM LOGIC → G

G

TEST TMS 9918 (VDP) PIN 36 COMPOSITE VIDEO. SET SCOPE AT 50mV/div AND 20μS/div TIME BASE

VDP PIN 36 SHOULD APEAR AS IN DIAGLAM ON RIGHT. THIS WAS TAKEN ON A WORKING SYSTEM WITH FRONT PANEL UP.



COMPOSITE VIDEO AND SYNC

NOTE: WE ARE TESTING HERE FOR SYNC AND BURST ONLY DON'T WORRY IF DATA SECTION IS NOT IDENTICAL TO THAT SHOWN.

VIDEO PRESENT ?

NO → VDP TESTS → H

YES

NEXT WE WANT TO SEE IF MICRO PROCESSOR (9900) IS SENDING DATA TO VDP - TO TRY AND ANSWER QUESTION, "IS PROBLEM ASSOCIATED WITH VIDEO CHIP, CIRCUIT OR THE SYSTEM LOGIC?" THIS IS LIKE TESTING IF A CALCULATOR HAS A PROBLEM WITH THE CALCULATOR CHIP OR THE DISPLAY DRIVER CHIP.

TEST 9918 PIN 14 (CHIP SELECT WRITE). THIS IS AN ACTIVE LOW SIGNAL. ITS PRESENCE AFTER DOING A SYSTEM POWER UP FOR AT LEAST A SECOND INDICATES 9900 IS TRYING TO COMMUNICATE TO VIDEO CHIP

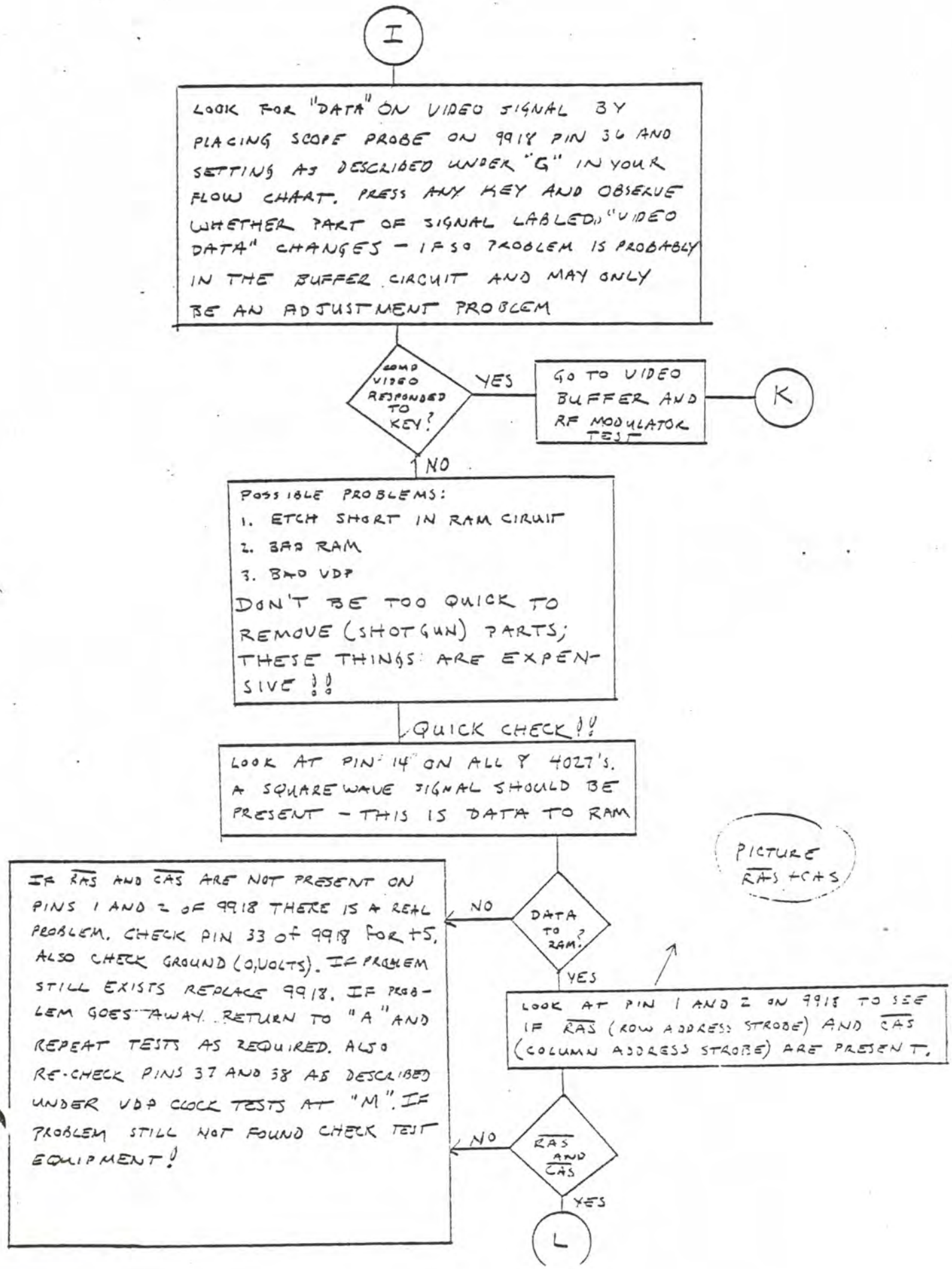
$\overline{CSW}$'s TO PIN 14 ?

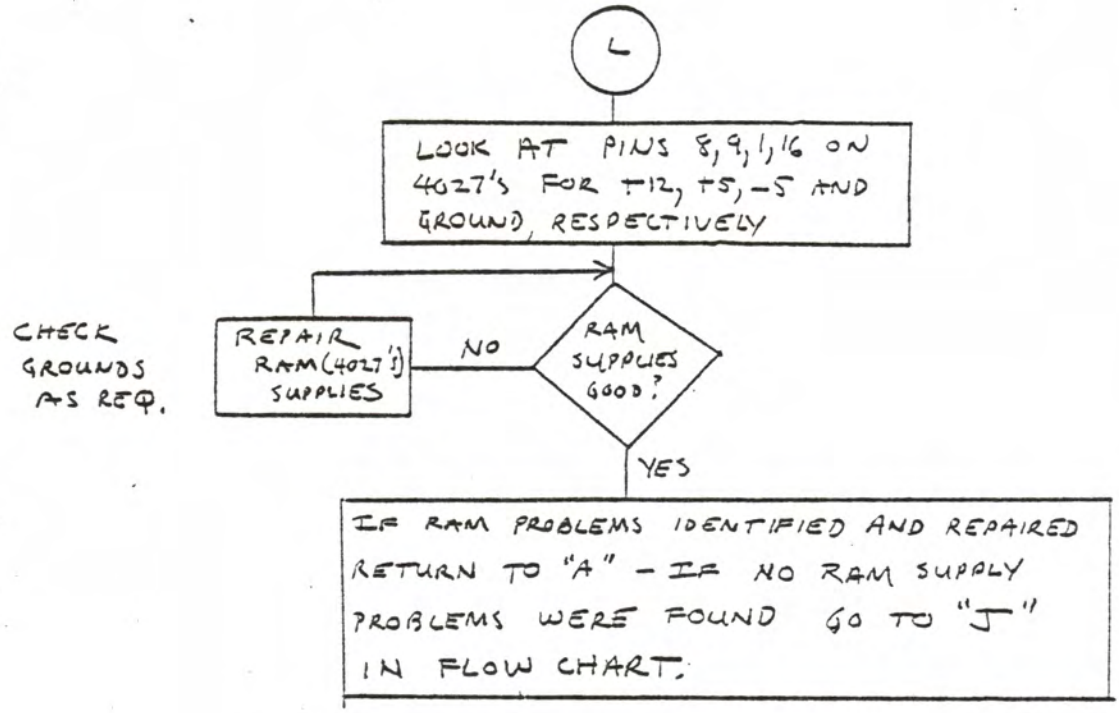
NO → THERE MAY STILL BE PROBLEMS WITH THE VIDEO CIRCUITRY BUT AT LEAST WE KNOW DATA (VIA $\overline{CS}$) IS NOT BEING SENT TO VDP. (INITIALLY) → CPU TESTS → J

YES

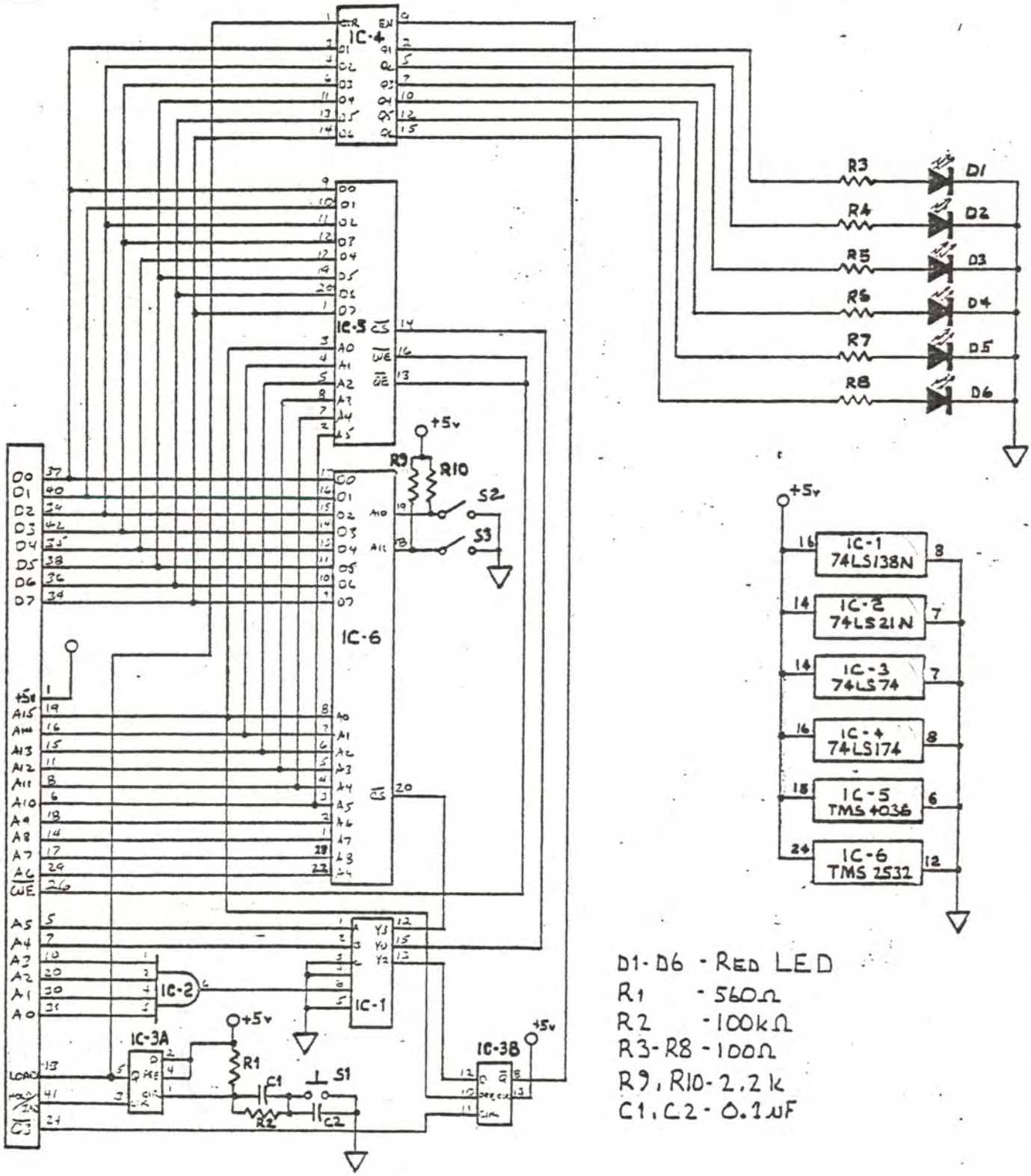
THERE MAY STILL BE A MAJOR PROBLEM WITH THE CPU LOGIC (9900) - BUT WE WANT TO CONTINUE TO TEST 9918 - OUR PROBLEM MAY VERY WELL BE IN THE VIDEO BUFFER, RF MODULATOR, VDP (9918) CHIP OR 4027 RAM

I


I
LOOK FOR "DATA" ON VIDEO SIGNAL BY PLACING SCOPE PROBE ON 9918 PIN 36 AND SETTING AS DESCRIBED UNDER "G" IN YOUR FLOW CHART. PRESS ANY KEY AND OBSERVE WHETHER PART OF SIGNAL LABLED "VIDEO DATA" CHANGES - IF SO PROBLEM IS PROBABLY IN THE BUFFER CIRCUIT AND MAY ONLY BE AN ADJUSTMENT PROBLEM
DOES VIDEO RESPONDED TO KEY?
YES
GO TO VIDEO BUFFER AND RF MODULATOR TEST
K
NO
POSSIBLE PROBLEMS:
1. ETCH SHORT IN RAM CIRUIT
2. BAD RAM
3. BAD VDP
DON'T BE TOO QUICK TO REMOVE (SHOTGUN) PARTS; THESE THINGS ARE EXPENSIVE !!
QUICK CHECK!!
LOOK AT PIN 14 ON ALL 8 4027's. A SQUARE WAVE SIGNAL SHOULD BE PRESENT - THIS IS DATA TO RAM
PICTURE RAS + CAS
DATA TO RAM?
NO
IF RAS AND CAS ARE NOT PRESENT ON PINS 1 AND 2 OF 9918 THERE IS A REAL PROBLEM. CHECK PIN 33 OF 9918 FOR +5, ALSO CHECK GROUND (0 VOLTS). IF PROBLEM STILL EXISTS REPLACE 9918. IF PROBLEM GOES AWAY RETURN TO "A" AND REPEAT TESTS AS REQUIRED. ALSO RE-CHECK PINS 37 AND 38 AS DESCRIBED UNDER VDP CLOCK TESTS AT "M". IF PROBLEM STILL NOT FOUND CHECK TEST EQUIPMENT!
YES
LOOK AT PIN 1 AND 2 ON 9918 TO SEE IF RAS (ROW ADDRESS STROBE) AND CAS (COLUMN ADDRESS STROBE) ARE PRESENT.
RAS AND CAS
NO
YES
L


L
LOOK AT PINS 8, 9, 1, 16 ON 4027's FOR +12, +5, -5 AND GROUND, RESPECTIVELY
RAM SUPPLIES GOOD?
NO
REPAIR RAM (4027's) SUPPLIES
CHECK GROUNDS AS REQ.
YES
IF RAM PROBLEMS IDENTIFIED AND REPAIRED RETURN TO "A" - IF NO RAM SUPPLY PROBLEMS WERE FOUND GO TO "J" IN FLOW CHART.

RAM TRAP SCHEMATIC

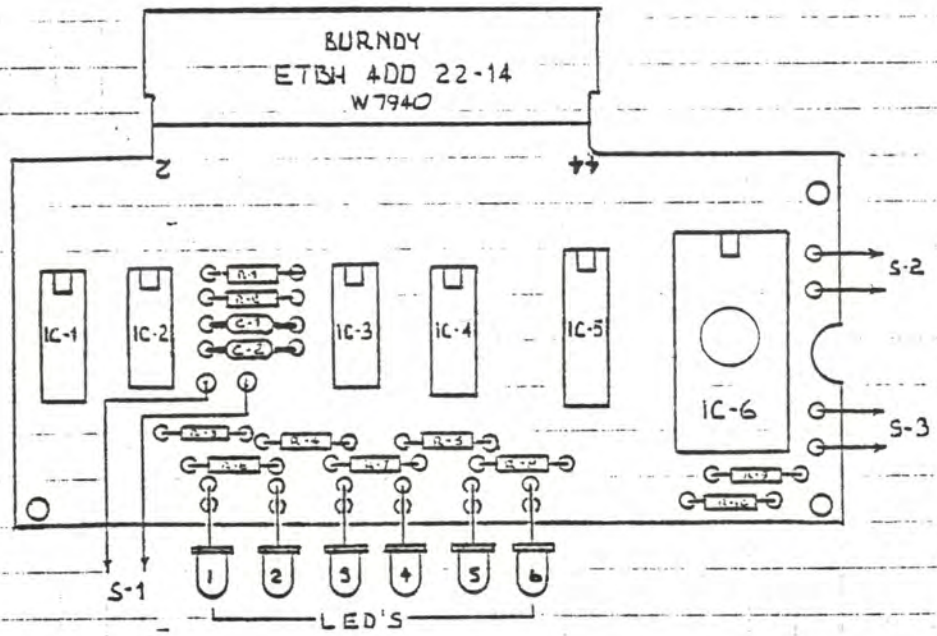


D1-D6 - RED LED
R1 - 560Ω
R2 - 100kΩ
R3-R8 - 100Ω
R9, R10 - 2.2k
C1, C2 - 0.1μF

BY: KMH 3·28·80

MAINFRAME RAM-TRAP

COMPONENT LAYOUT:

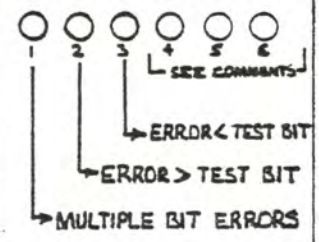
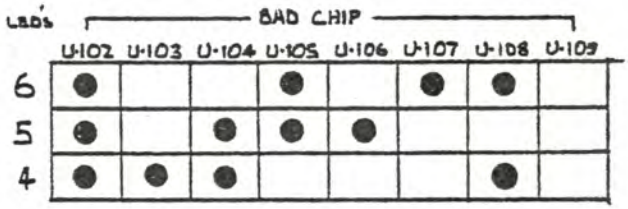
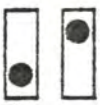
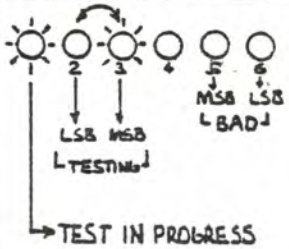
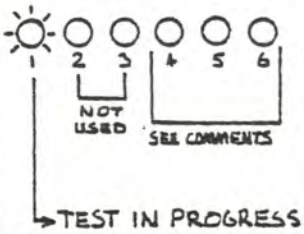
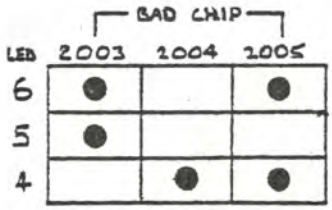


PARTS LIST:

C-1, C-2	0.1 nF CAPACITORS	R-1	560 Ω	ALL RESISTORS ARE ¼ WATT 5%
IC-1	74LS138N	R-2	100 kΩ	
IC-2	74LS21N	R-3 → R-8	100 Ω	
IC-3	74LS74AN	R-9, R-10	2.2 kΩ	
IC-4	74LS174N	S-1	SPST PUSHBUTTON SWITCH (MOMENTARY N.O.)	
IC-5	TMS 4036-2NL	S-2, S-3	SPST TOGGLE SWITCHES	
IC-6	2532 (EPROM)			

BY: [redacted] 3-4-80

RAM TRAP OPERATING INSTRUCTIONS

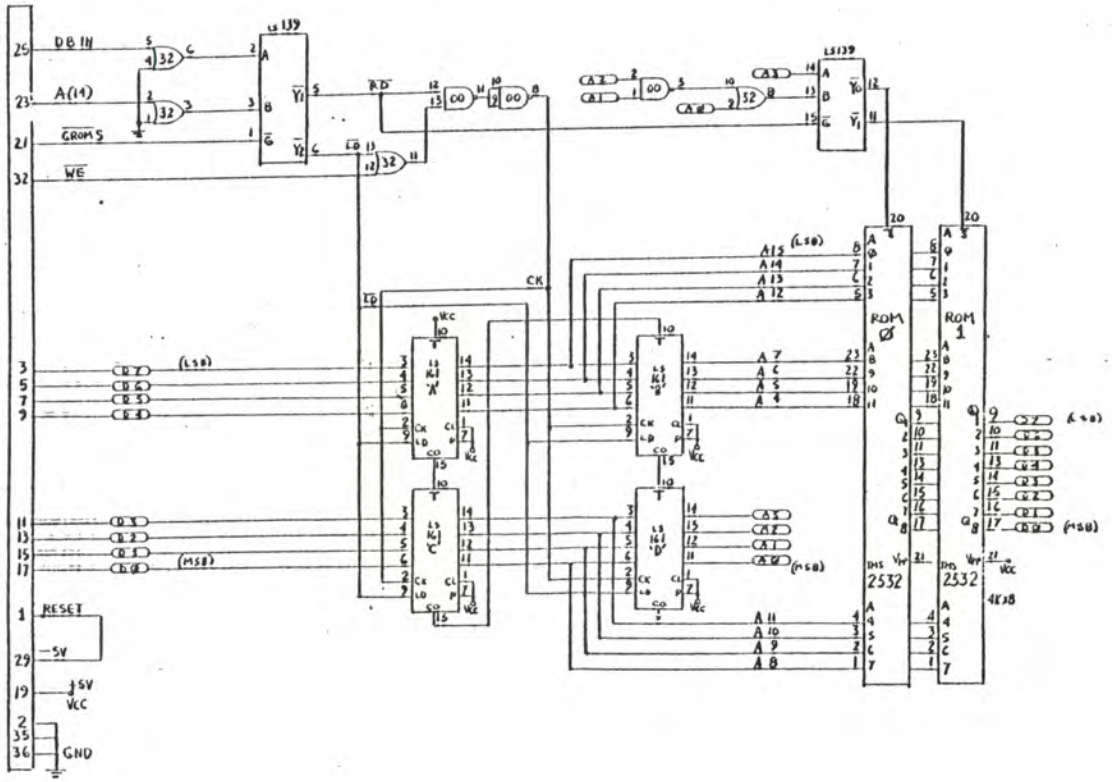
TEST FUNCTION	SWITCH POSITION	INDICATORS	COMENTS
4116's U102 → U109			
6810's U608, U609			2ND & 3RD INDICATORS SHOULD ALTERNATE SLOWLY. 5TH INDICATOR SHOWS MSB ERROR 6TH INDICATOR SLOWS LSB ERROR
2003 2004 2005			

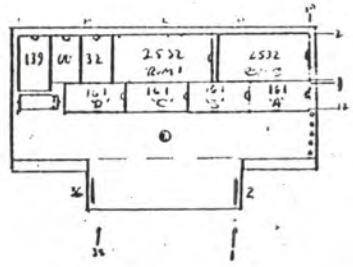
BEFORE EACH TEST MAKE SURE THE UNIT UNDER TEST IS SWITCHED "OFF."

START UP PROCEDURE:

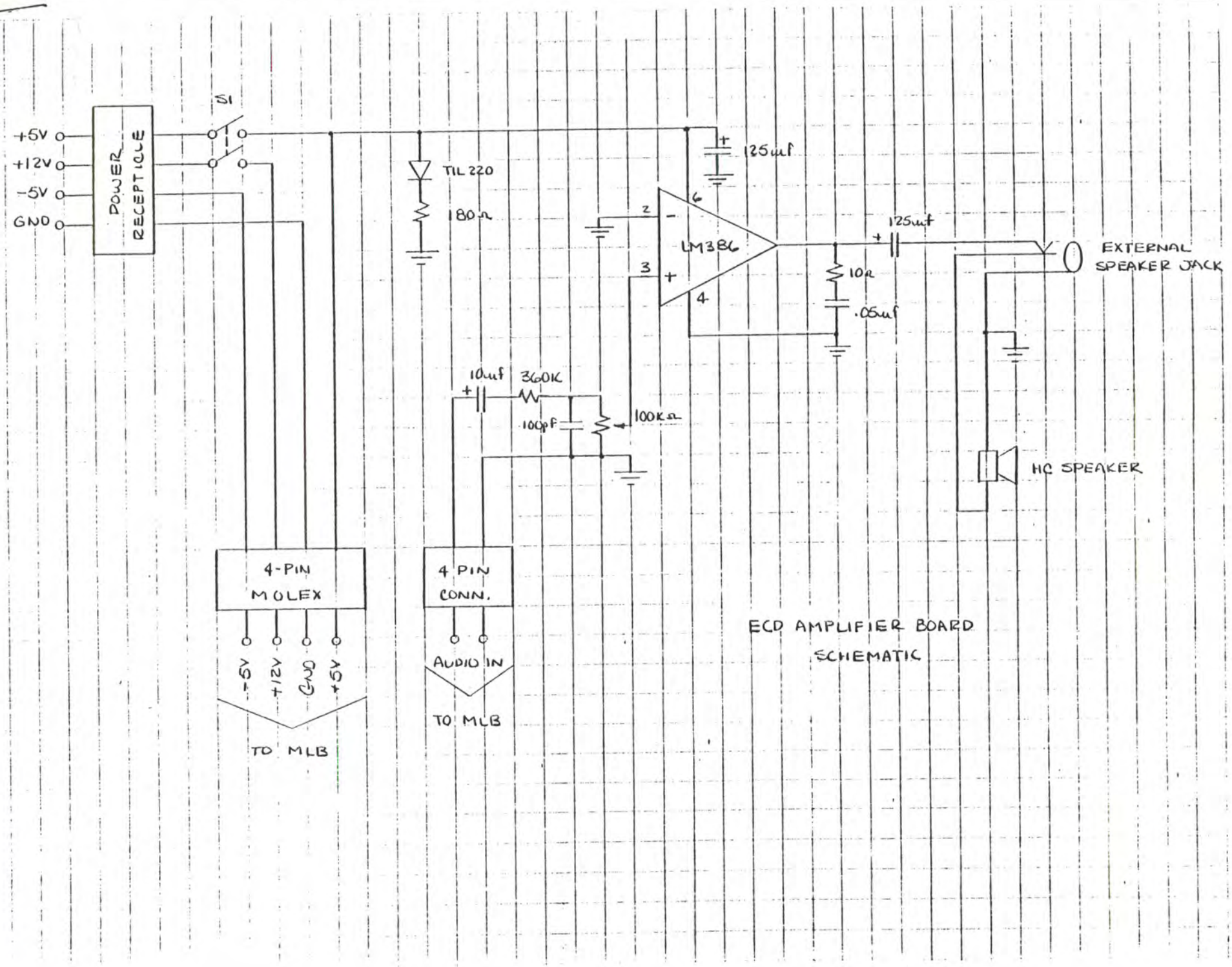
1. TURN UNIT TO BE TESTED "OFF"
2. INSERT RAM TRAP
3. SELECT TEST MODE ON RAM TRAP
4. TURN "ON" UNIT TO BE TESTED
5. PRESS LOAD SWITCH

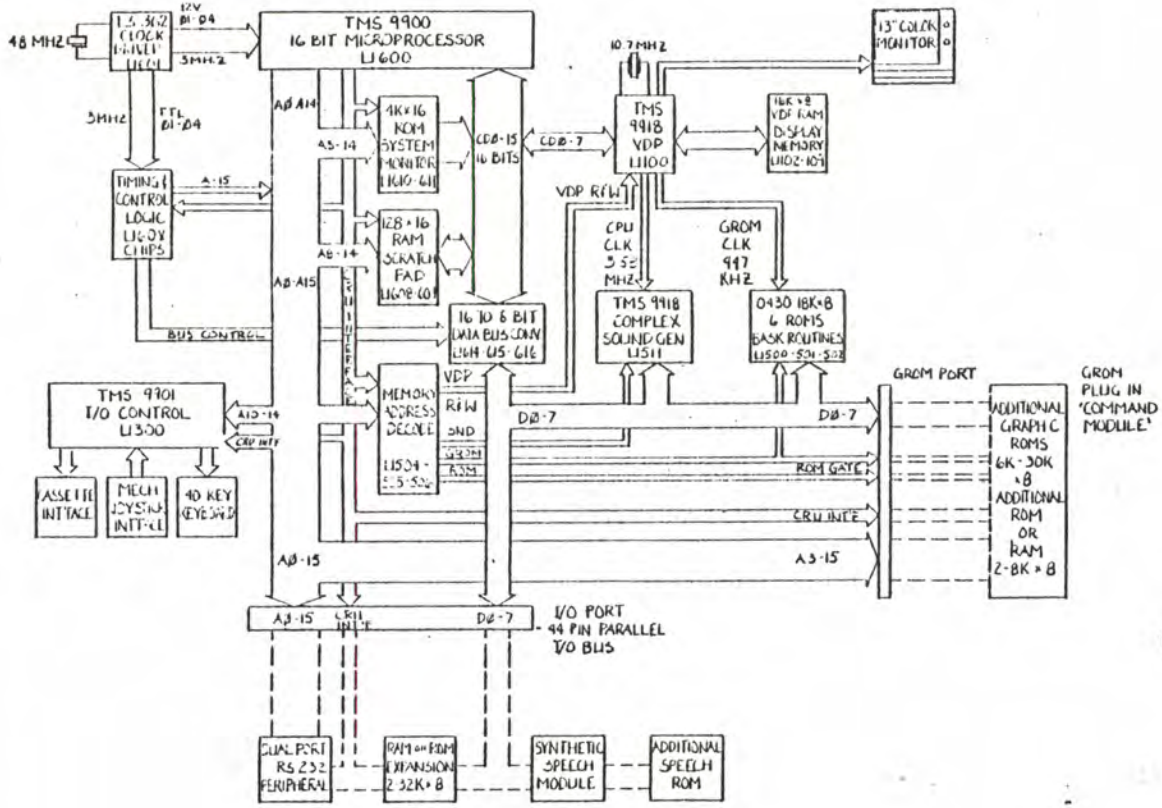
BY: KMM 3-31-80





MATERIAL		
PROCESSED		
KC Davis 6-25-79		XXX ± .010 XX ± .020 X ± .030
		TEXAS INSTRUMENTS INCORPORATED SEMICONDUCTOR GROUP
		01295
EGROM SIMULATOR SINGLE PLUG IN UNIT.		
—	C	SK1017 ASSY
		1/1


+5V
+12V
-5V
GND
POWER RECEPTICLE
S1
TIL 220
180Ω
125μf
LM386
2
6
3
4
125μf
10Ω
.05μf
EXTERNAL SPEAKER JACK
10μf
360K
100pF
100KΩ
HC SPEAKER
4-PIN MOLEX
-5V
+12V
GND
+5V
TO MLB
4 PIN CONN.
AUDIO IN
TO MLB
ECD AMPLIFIER BOARD SCHEMATIC



NOTE: These drawings were obtained and updated by Deaton Smith on 3/25/80. If any errors to these drawings are noted please relay to Deaton so the correction can be made and new drawing run.

Thanks, Deaton
3-25-80

Changes:

1. RFI
2. CASSETTE MOTOR DRIVE
3. Deletion of Phone Jack. At audio out CKT
4. Addition of Caps in P.S.

PRELIMINARY
FOR INFORMATION ONLY
DATE 2-22-80

PARTS LIST

ITEM NO	PART OR IDENTIFYING NUMBER	NOMENCLATURE OR DESCRIPTION	REMARKS

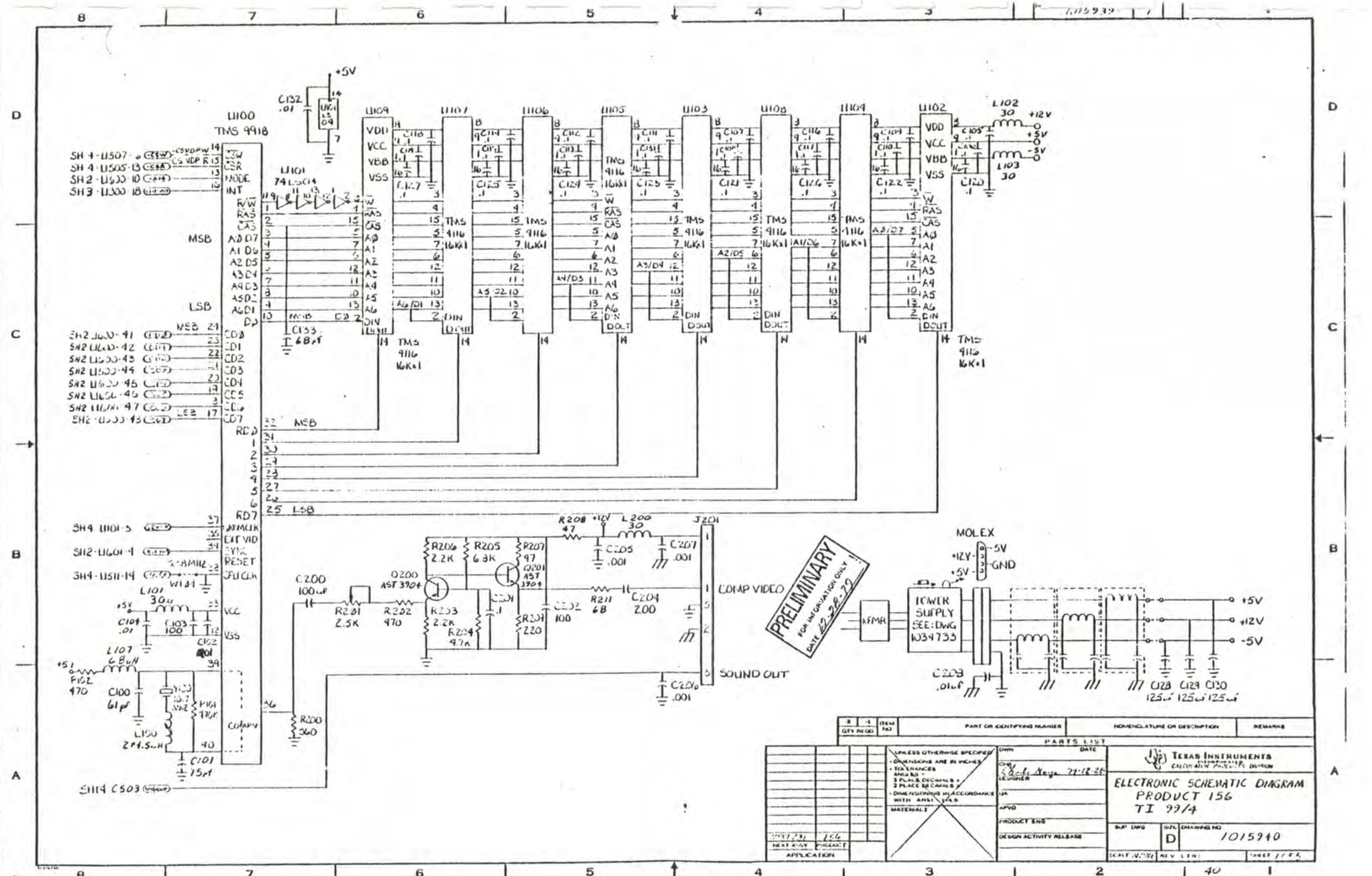
TEXAS INSTRUMENTS
CALCULATOR PRODUCTS DIVISION

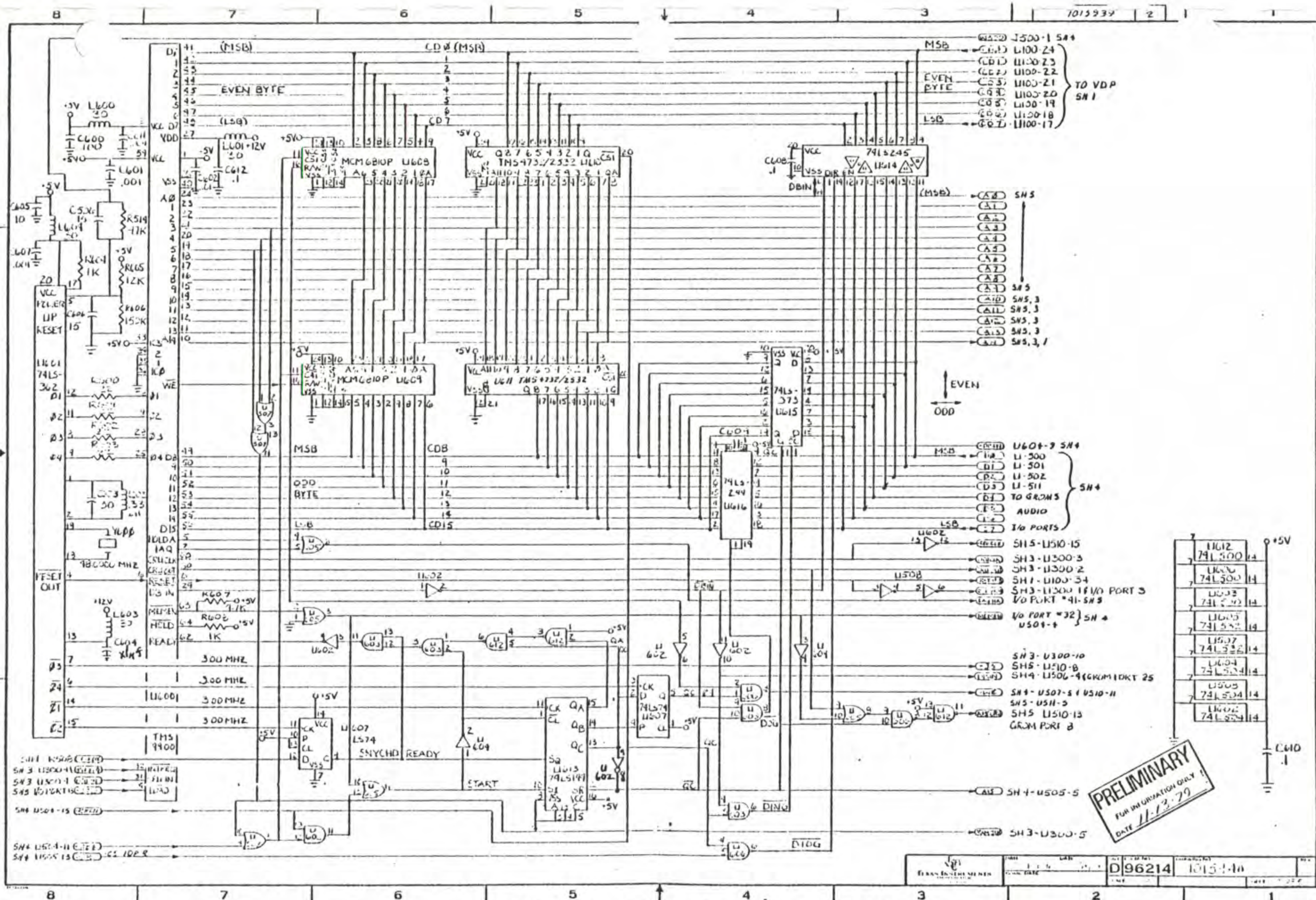
BLOCK DIAGRAM
TI 99/4

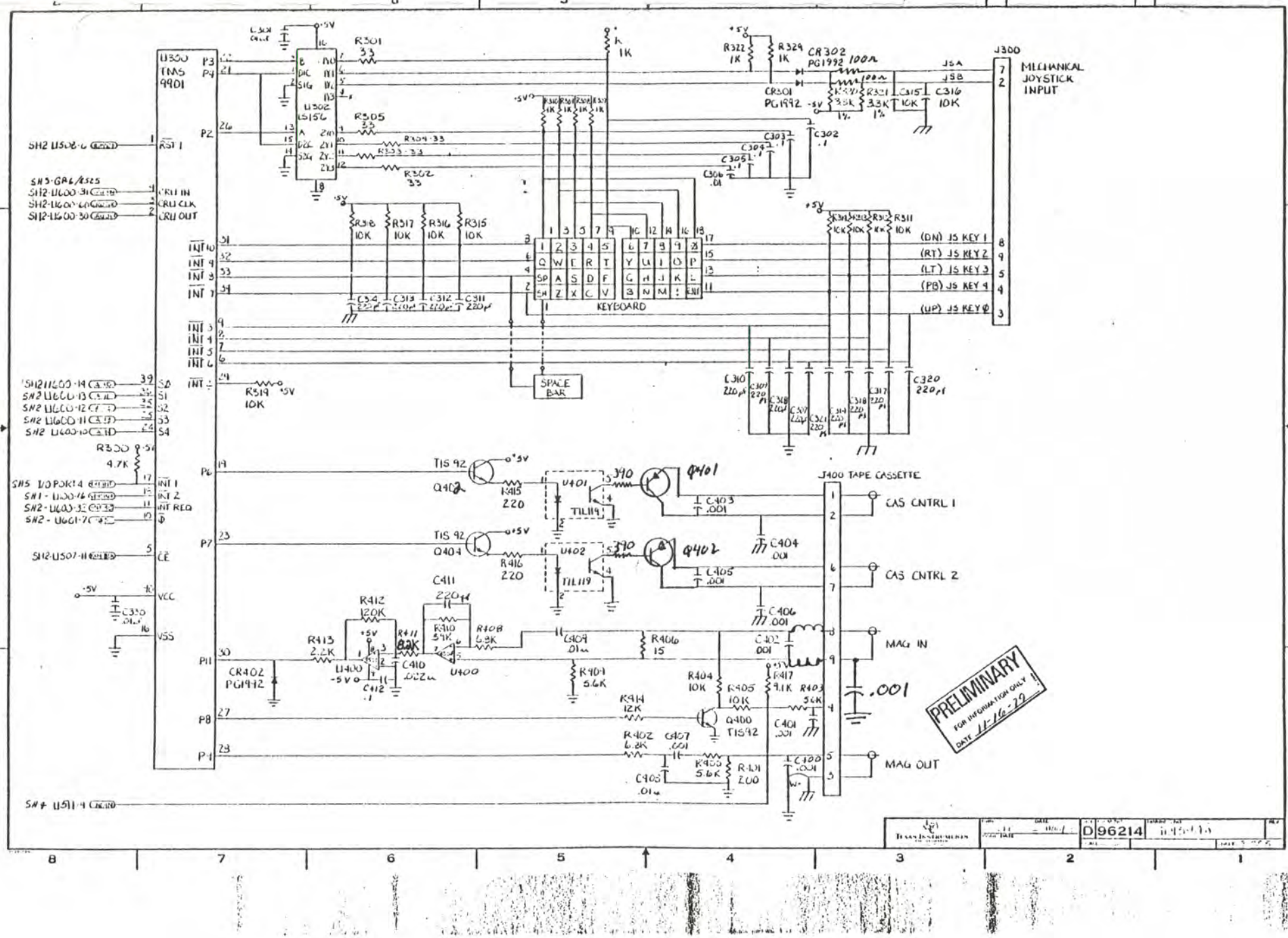
SIZE D

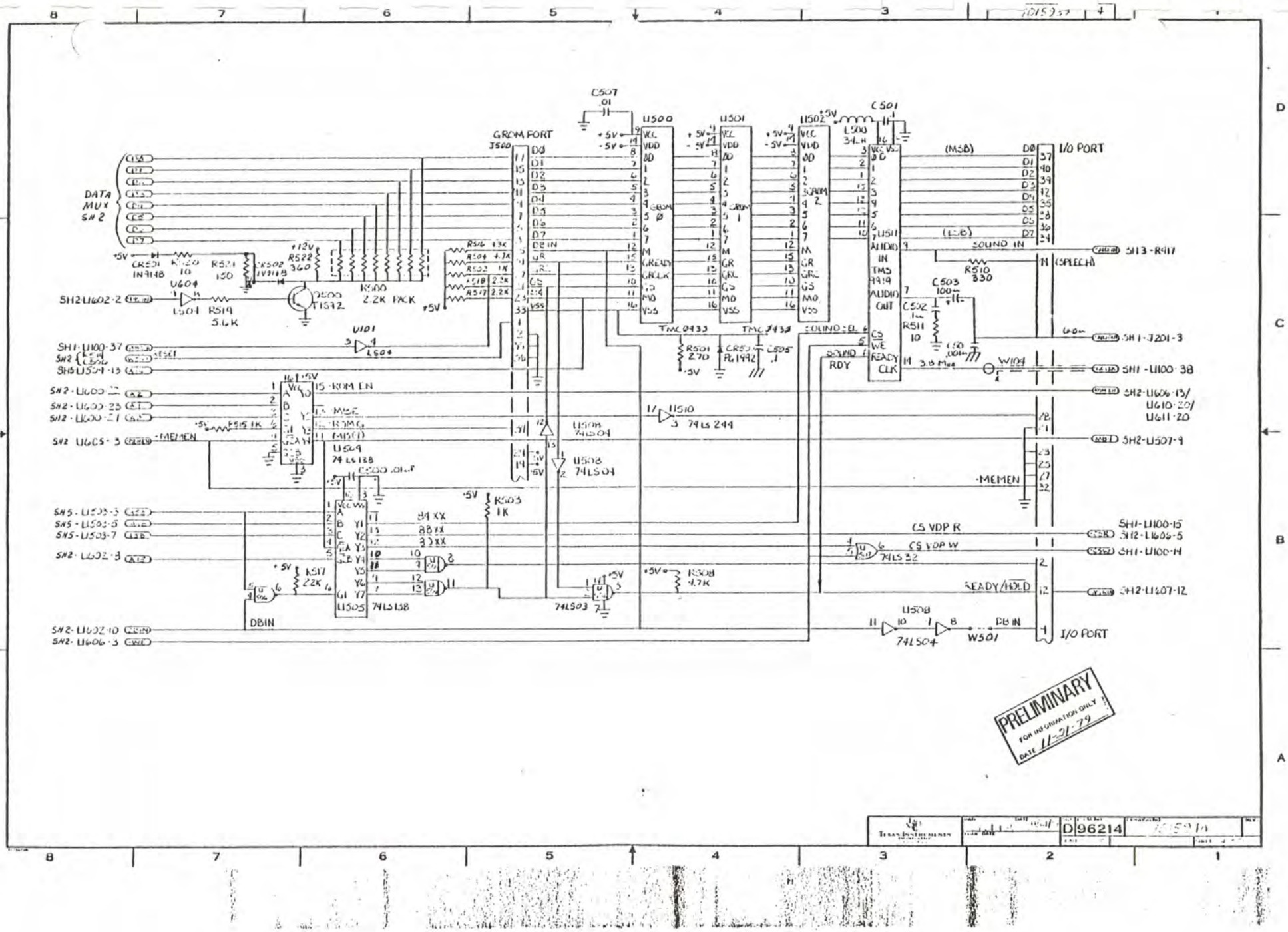
SHEET 1 OF 1

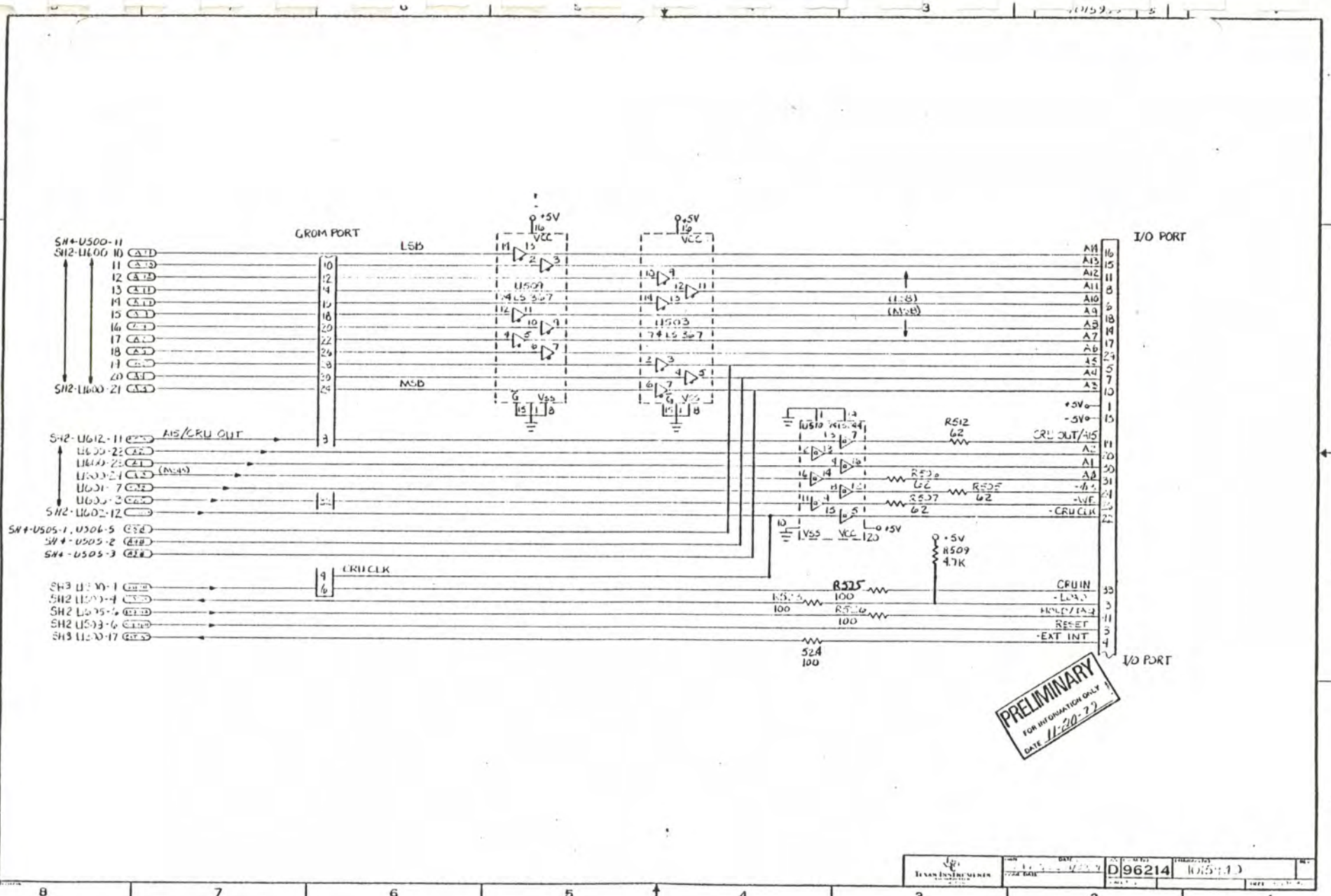
CLASS CODE: 90


U100
TMS 9918
U101
74LS04
U109
U107
U106
U105
U103
U108
U104
U102
TMS 4116 16K×1
MSB
LSB
COMP VIDEO
SOUND OUT
J201
MOLEX
POWER SUPPLY SEE: DWG 1034733
XFMR
PRELIMINARY
FOR INFORMATION ONLY
DATE 12-28-79
+5V
+12V
-5V
GND
PARTS LIST
TEXAS INSTRUMENTS
ELECTRONIC SCHEMATIC DIAGRAM
PRODUCT 156
TI 99/4
D
1015940

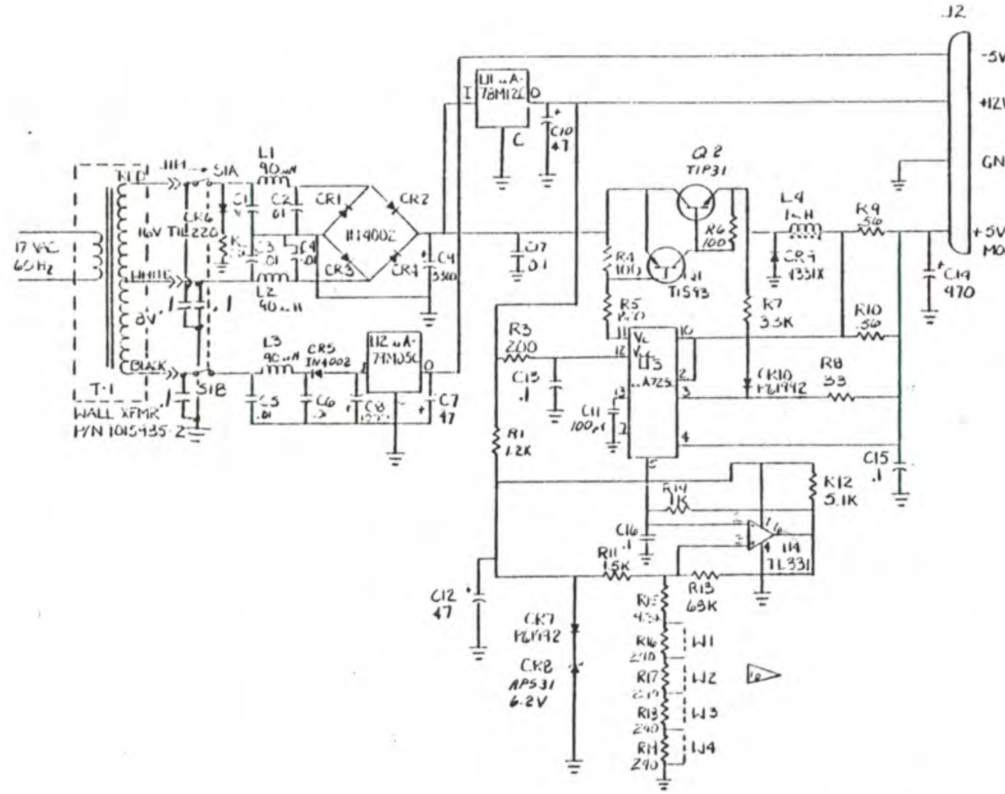

1015339
MCM6810P U608
MCM6810P U609
TMS4732/2532 U610
TMS4732/2532 U611
74LS245 U614
74LS373 U615
74LS244 U616
74LS74 U607
74LS161 U613
74LS362 U601
TMS 9900
TO VDP SH 1
TO GROMS
AUDIO
I/O PORTS
EVEN BYTE
ODD BYTE
EVEN
ODD
SNYCHD
READY
START
3.00 MHZ
PRELIMINARY
FOR INFORMATION ONLY
DATE 11-13-79
D96214
1015348


U300 TMS 9901
MECHANICAL JOYSTICK INPUT
KEYBOARD
SPACE BAR
(DN) JS KEY 1
(RT) JS KEY 2
(LT) JS KEY 3
(PB) JS KEY 4
(UP) JS KEY 0
J400 TAPE CASSETTE
CAS CNTRL 1
CAS CNTRL 2
MAG IN
MAG OUT
U400
U401
U402
Q400
Q401
Q402
CR301 PG1992
CR302 PG1992
CR402 PG1992
SPACE BAR
PRELIMINARY
FOR INFORMATION ONLY
DATE 11-16-79
D96214


PRELIMINARY
FOR INFORMATION ONLY
DATE 11-21-79
D96214


GROM PORT
LSB
MSB
I/O PORT
+5V
VCC
VSS
U500
U501
U502
U503
74LS367
A15/CRU OUT
(MSB)
CRU CLK
R512
62
R509
4.7K
R525
100
R524
100
CRU OUT/A15
CRUIN
-LOAD
HOLD/IAQ
RESET
-EXT INT
-MEMEN
-WE
-CRUCLK
PRELIMINARY
FOR INFORMATION ONLY
DATE 11-20-79

NOTES - UNLESS OTHERWISE SPECIFIED:
1. CAPACITANCE VALUES ARE IN MICROFARADS
2. DIODES ARE PG 1992
3. INDUCTANCE VALUES ARE IN MICROHENRYS
4. RESISTANCE VALUES ARE IN OHMS
5. ALL RESISTORS ARE 1/4 W ±5%
6. CUT JUMPERS TO OBTAIN 5.0 V ±5%. EACH CUT EQUALS .035 V INCREASE



HIGHEST REFERENCE DESIGNATION USED			
R19	C17	CR10	L4

REFERENCE DESIGNATIONS NOT USED

QTY REQD	ITEM NO	PART OR IDENTIFYING NUMBER	NOMENCLATURE OR DESCRIPTION	REMARKS

PARTS LIST

UNLESS OTHERWISE SPECIFIED: DIMENSIONS ARE IN INCHES; TOLERANCES: ANGLES ±; 3 PLACE DECIMALS ±; 2 PLACE DECIMALS ±; DIMENSIONING IN ACCORDANCE WITH ANSI Y14.5
MATERIALS

DWN: [illegible] DATE 79/11/1
CHK / DESIGNER: [illegible] 79-12-28
QA
APVD
PRODUCT ENG
DESIGN ACTIVITY RELEASE

APPLICATION: NEXT ASSY | PRODUCT

TEXAS INSTRUMENTS
CALCULATOR PRODUCTS DIVISION

ELECTRONIC SCHEMATIC DIAGRAM CONSOLE POWER SUPPLY TI 99/4

SIZE D DRAWING NO 1034733
SCALE | REV LTR | SHEET
CLASS CODE: 40

REVISIONS: ZONE | LTR | DESCRIPTION | DATE | APPROVED

D 1034733